Fuzzy Controlled Parallel AC-DC Converter for PFC

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Abstract. *Paralleling of converter modules is a well-known technique that is often used in medium-power applications to achieve the desired output power by using smaller size of high frequency transformers and inductors. In this paper, a parallel-connected single-phase PFC topology using flyback and forward converters is proposed to improve the output voltage regulation with simultaneous input power factor correction (PFC) and control. The goal of the control is to stabilize the output voltage of the converter against the load variations. The paper presents the derivation of fuzzy control rules for the dc/dc converter circuit and control algorithm for regulating the dc/dc converter. This paper presents a design example and circuit analysis for 200 W power supply. The proposed approach offers cost effective, compact and efficient AC/DC converter by the use of parallel power processing. MATLAB/SIMULINK is used for implementation and simulation results show the performance improvement.*

Keywords

Flyback converter, PFC, power conversion, fuzzy control.

1. Introduction

A number of power factor correction circuits have been developed recently [1], [2], [3], [4] and [5]. Normally a boost converter is employed for PFC with DC/DC stage to improve performance or a flyback converter is used to reduce the cost. Although both boost converter and flyback converter are capable for PFC applications [6], the main difficulty in two-stage scheme employing a PFC boost and a DC/DC converter is the high cost and lower efficiency. However, single-stage method using the simplest flyback converter is not able to tightly regulate the output voltage.

Paralleling of converter power modules [7] is a well-known technique that is often used in high-power applications to achieve the desired output power with smaller size power transformers and inductors [10]. Since magnetics are critical components in power converters because generally they are the size-limiting factors in achieving high-density and/or low-profile power supplies, the design of magnetics becomes even more challenging for high-power applications that call for high power-density and low-profile packaging. Instead of designing large-size centralized magnetics that handle the entire power, low-power distributed high density low-profile magnetics can be utilized to handle the high processing power, while only partial load power flow through each individual magnetics [10], [11].

In addition to physically distributing the magnetics and their power losses and thermal stresses, paralleling also distributes power losses and thermal stresses of the semiconductors due to a smaller power processed through the individual paralleled power stages. As a result, paralleling is a popular approach to eliminating "hot spots" in power supplies. In addition, the switching frequencies of paralleled, lower-power power stages may be higher than the switching frequencies of the corresponding single, high-power processing stages because lower-power, faster semiconductor switches can be used in implementing the paralleled power stages. Consequently, paralleling offers an opportunity to reduce the size of the magnetic components and to achieve a low-profile design for high power applications.

Without increasing the number of power stages and control-circuit components, the transformer magnetics can be distributed by direct transformer paralleling. Not only that transformer paralleling distributes the processed power in each magnetics components, but also their power losses and thermal stresses are distributed at the same time. However, current sharing among the paralleled transformers needs to be maintained to ensure power balance.

In its basic form, the interleaving technique can be viewed as a variation of the paralleling technique, where the switching instants are phase-shifted within a switching period [12]. By introducing an equal phase shift between the paralleled power stages, the total inductor current ripple of the power stage seen by the

output filter capacitor is lowered due to the ripple Cancellation effect [12].

The goal of the proposed PFC scheme is to reduce the passive component size, to employ lower rated semiconductor, and to improve total efficiency. Simulation results show that the proposed topology is capable of offering good power factor correction and fast dynamic response.

2. PFC Cells

2.1 Two Stage PFC Approach

A two-stage scheme shown in Fig. 1 is mainly employed for the switching power supplies since the boost stage can offer good input power factor with low total harmonic distortion (THD) and regulate the dc-link voltage and the DC/DC stage is able to obtain fast output regulation without low frequency ripple due to the regulated dc-link voltage [13]. These two power conversion stages are controlled separately. However, two-stage scheme suffers from higher cost, complicated control, low-power density, and lower efficiency.

2.2 Single Stage PFC Approach

For low power applications, where cost is a dominant issue, a single-stage scheme using the flyback converter Fig. 2 is more attractive than a two-stage scheme.

2.3 Parallel PFC Approach

At higher power levels, since it may be beneficial to parallel two or more DC/DC converters rather than using a single higher power unit, a parallel-connected scheme is proposed as shown in Fig. 3. This approach can offer

fast output voltage regulation and high efficiency. The forward converter with DC/DC stage can offer good output voltage regulation due to the pretty dc input voltage and the flyback converter with AC/DC PFC stage fulfills input current regulation to obtain highly efficient power factor.
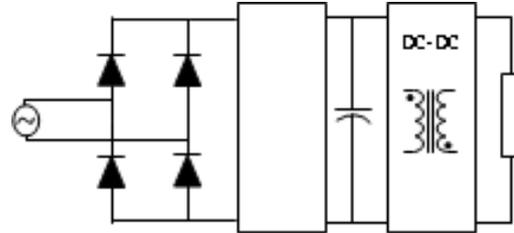
Fig. 1: Two-Stage PFC.
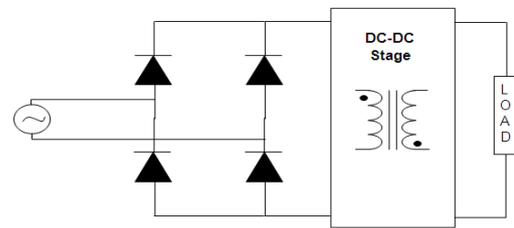
Fig. 2: Single stage PFC.
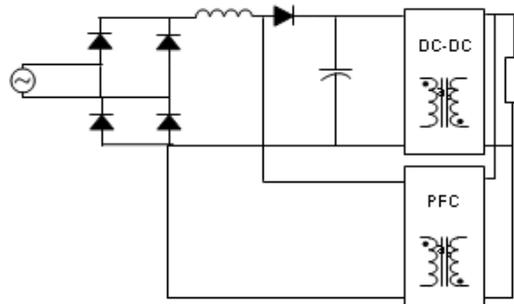
Fig. 3: Proposed parallel-connected single-phase PFC scheme.
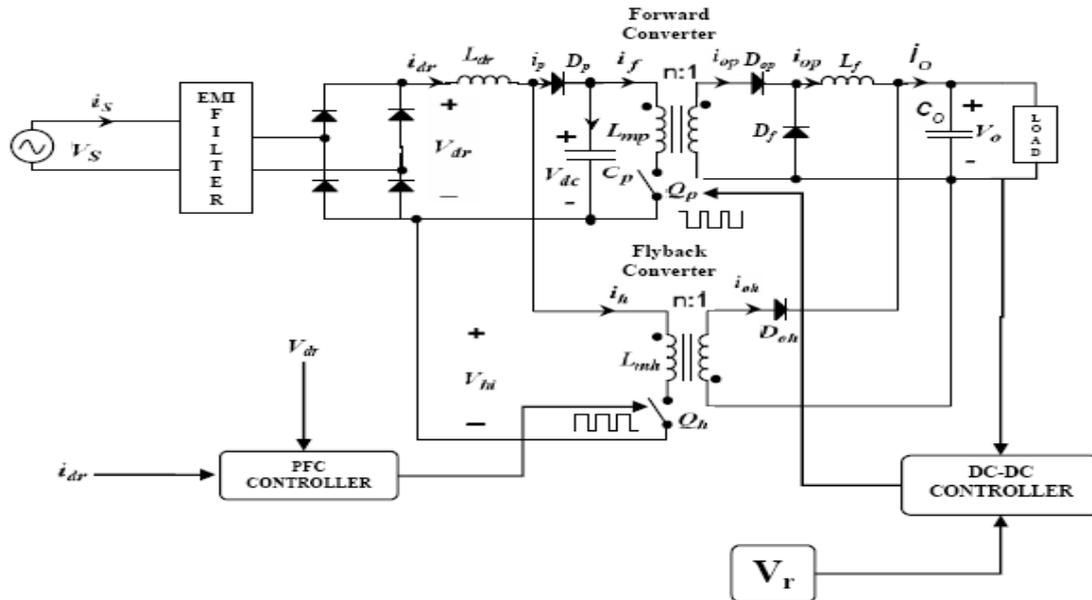
Fig. 4: Parallel-connected single-phase PFC scheme.

3. Proposed Parallel PFC Scheme

Figure 4 shows the proposed parallel-connected PFC scheme which employs a diode rectifier, dc-link capacitor, forward converter and flyback converter. The function of a forward converter with an electrolytic capacitor is to support output voltage regulation.

A flyback converter fulfills the function of power factor correction by making input current sinusoidal and regulating dc-link voltage. The operation of the flyback converter is given in this paragraph considering that the forward converter operates ideally. The PFC Cell (forward converter) operates with continuous conduction mode in both an input inductor and a flyback transformer. The dc-link voltage in this scheme:

$$V_{dc} = \sqrt{2} \cdot V_s . \qquad (1)$$

The transfer function of the flyback converter is expressed by defining a conversion ratio as the ratio of the dc output voltage to the input voltage:

$$M = \frac{V_o}{V_{dr}} = \frac{D}{D(1-n)} , \qquad (2)$$

where, D is the duty ratio of the switch Q_h, n (=N_p/N_s), is defined as the ratio of N_p to N_s, and N_p and N_s denote the number of turns of primary and secondary side, respectively. To analyze the circuit parameters, basic equations for voltages and currents are given by:

$$i_{dr} = i_p + i_h , \qquad (3)$$

$$V_{Ldr} = L_{dr} \frac{di_r}{dt} , \qquad (4)$$

$$V_{hi} = V_{dr} - V_{Ldr} , \qquad (5)$$

$$V_{h1} = V_{hi} - V_{Qh} , \qquad (6)$$

where i_{dr}, i_p, and i_h are the rectified, DC/DC Cell, and PFC Cell input currents on dc side. V_{Ldr}, V_{hi}, V_{hi}, V_{dr} ,V_{h1}, V_{Qh}, and V_o and are the input inductor, flyback converter input, rectified input, transformer primary winding, switch, and output voltages, respectively. Since the two input currents, i_p and i_h, are interleaved, input current, i_{dr}, ripple can be significantly reduced.

The operational sequences are as follows:

- $t_0.t_1$: As shown in Fig. 5(a) The current of flyback transformer does not flow simultaneously in both windings. When the switch Q_h is turned *ON* at t_o, V_Q becomes zero and diode D_{oh} is turned *OFF* with a reverse bias. The voltage across the diode D_{oh} equals to $V_o + V_{hi}/n$. Energy, $L_{mh}I^2$, is charged in the magnetic field in the primary winding of the flyback transformer. Primary current, i_h, ramps up from the remaining magnetizing current and reaches I_{dr} with the slope, (V_{hi}/L_{mh}), i_p decreases with a slow current tail, and slowly decreases until i_p reaches zero. At the same time the forward converter switch Q_p is *OFF* because, as the switch Q_h is *ON* the potential at he junction of diode D_p and input inductor L_{dr} i.e. $V_{Ldr} > V_{hi}$, the diode D_p is reverse biased. The diode D_{op} is also reverse biassed due to the polarity of the forward transformer and a negative voltage of -nV_o. The voltage across the output inductor is $V_L = -V_o$ and the inductor current i_{Lf} decreases and i_{Lf} along with i_{oh}, circulates through diode D_f, and supplied to load.
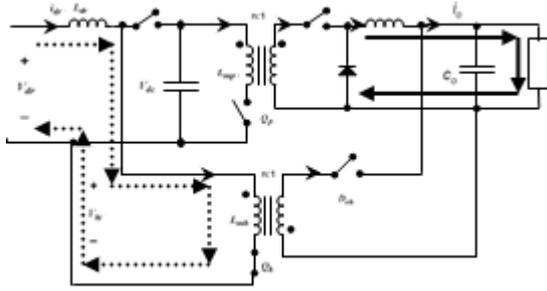
Fig. 5(a): Forward converter switch Q_p is *OFF* and flyback converter switch Q_h is *ON*.

- t_1_t_2: The primary current of flyback converter increases by $V_{dr}/(L_{mh} + L_{dr})$. The voltage across switch Q_p decreases from $2V_{dr}$ to V_{dr}. The input inductor current ramps up to till switch Q_h is *OFF*.
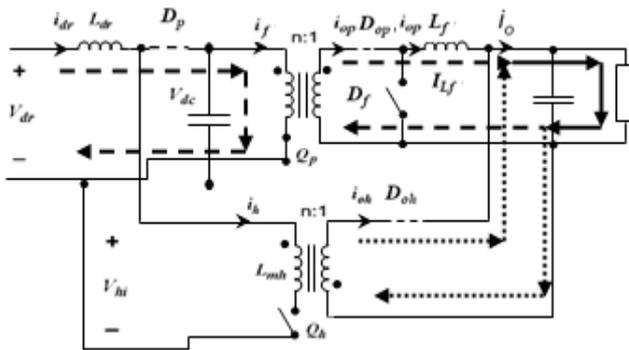
Fig. 5(b): Forward converter switch Q_p is *ON* and flyback converter switch Q_h is *OFF*.

- **t_2_t_3:** As shown if Fig. 5(b), when the switch Q_h is turned *OFF*, D_{oh} is turned *ON* with forward bias. The current in the primary winding ceases to flow. The stored energy is transferred to the secondary winding. At this time, the switch voltage, V_{Qh}, becomes $V_{hi}+nV_o$, i_p becomes i_{dr} and decreases depending on input voltage, and the secondary current decreases with the slope (n^2V_o/L_{mh}). When the switch Q_p is *ON*, the diode D_p is forward biased because the potential at junction between the diode and inductor is $V_{Ldr}<V_{hi}+nV_o$. The primary current of forward transformer ramps up and the energy stored in the primary winding is instantaneously transferred to secondary, because of the same polarity of the forward transformer. The diode D_{op} is forward biassed and diode D_f is reversed biassed. The output inductor current i_{Lf} increases along with i_{oh} which is delivered to load.

The current slope through the magnetizing inductor when the switch Q_h is turned off is given as:

$$\Delta i_{mh} = -\frac{nV_o}{L_{mh}}T_{off} ,$$ (7)

where, T_{off} is the turn-off time. Similarly, the change of the flyback converter input current i_p through a diode is:

$$\Delta i_p = -\frac{Vdc - Vdr}{L_{dr}}T_{off} .$$ (8)

Based on two slopes of i_{mh} and i_p, the tailed diode current mode in which the diode current has current tail, when the slope of i_{mh} is greater than that of i_p:

$$v_{dr} > \frac{L_{mh}Vdc - nV_oL_{dr}}{L_{mh}} .$$ (9)

In continuous conduction input inductor current mode, when the MOSFET is switched on, the diode D_p is forced into reverse recovery at a high rate of change in the diode current i_p. In this tailed mode operation, however, the diode current slowly decreases so that the reverse recovery effect can be minimized.

To analyze the flyback converter operation, an open loop duty ratio is obtained from (2) as:

$$D_{open,h} = \frac{nV_o}{v_{dr} + nV_o} ,$$ (10)

where, input voltage $v_{dr} = \sqrt{2}V_s|Sin\omega t|$:

$$i_h = \frac{i_{dr}T_{on}}{T_s} = D.i_{dr} ,$$ (11)

$$i_p = (1-D).i_{dr} ,$$ (12)

where, input current $i_{dr} = \sqrt{2}I_s|Sin\omega t|$.

Therefore, two currents can be obtained:

$$i_h = \frac{\sqrt{2}nV_oI_s|Sin\omega t|}{\sqrt{2}V_s|Sin\omega t| + nV_o} ,$$ (13)

$$i_p = \sqrt{2}I_s|Sin\omega t|\left\{1 - \frac{nV_o}{\sqrt{2}V_s|Sin\omega t| + nV_o}\right\} .$$ (14)

$$= \sqrt{2}I_s|Sin\omega t| - i_h$$

The instantaneous powers through the diode D_p and the transformer T_2 are calculated by using the input inductance and the magnetizing inductance:

$$P_{p,pu} = \frac{L_{mh} + L_{dr}}{2L_{mh} + L_{dr}}[p.u],$$ (15)

$$P_{h,pu} = \frac{L_{mh}}{2L_{mh} + L_{dr}}[p.u],$$ (16)

where, L_{mh} and L_{dr} denote the magnetizing inductance of T_2 and input inductance, respectively, and the input total power $P_{in,pu} = P_{p,pu} + P_{h,pu} = 1[p.u]$. On the other hand by employing the open loop duty ratio $D_{open,\,h}$, two instantaneous powers can be derived by:

$$P_p = V_{dc}.i_p = \sqrt{2}V_s\left[\sqrt{2}I_s|Sin\omega t| - i_h\right],$$ (17)

$$P_h = P_{in} - P_p, \qquad (18)$$

where $P_{in} = V_s I_s \{1 - \cos 2\omega t\}$. The relations between two inductances and two input average powers of two converters are expressed as:

$$\frac{L_{mh} + L_{dr}}{L_{mh}} = \frac{P_{p,ave}}{P_{h,ave}}, \qquad (19)$$

$$L_{dr} = L_{mh} \left\{ \frac{P_{p,ave}}{P_{h,ave}} - 1 \right\}. \qquad (20)$$

The output currents of the two cells are given by turns ratio:

$$\begin{aligned} i_{op} &= n.i_f \\ i_{oh} &= n.i_h \end{aligned}. \qquad (21)$$

Since the output load current i_o may contain only dc and switching frequency components, the harmonic contents for the primary current of the flyback converter-I is expressed as:

$$i_o = i_{op} + i_{oh} = \frac{V_s I_s}{V_o}, \qquad (22)$$

$$i_{f,x} = i_{h,x}, \qquad (23)$$

where, x = (2 , 4, 6, etc.) is harmonic order. From (23), the dc-link capacitor current can be estimated as a second harmonic:

$$i_{dc,2} = -(i_{p,2} + i_{h,2}) \cos 2\omega t. \qquad (24)$$

Therefore, the voltage ripple of the dc-link capacitor is obtained as:

$$V_{dc,ripple} = -\frac{i_{p,2} + i_{h,2}}{2\omega C_p} \sin 2\omega t, \qquad (25)$$

where, Cp is the capacitance of the dc-link capacitor.

4. Converter Controllers

To control the proposed approach, two control stages are required for PFC and output voltage regulation as shown in Fig. 6. Flyback converter is regulated by a conventional PFC controller which consists of inner input current loop and outer dc-link voltage [13] to obtain high power factor. DC-link voltage is 1,414*V_s, which is better to reduce the voltage across drain-source of MOSFET Q_p. Based on the PFC controller, a feed-forward control block is added to improve input current shape. Since the open loop duty ratio $D_{open,h}$ of the PFC cell is calculated from (10), the final duty ratio for the switch gate input is obtained as

$$D_h = D_{open,h} + D_{pi}, \qquad (26)$$

where D_{pi}, is the closed loop duty ratio obtained from S-R flip flop current controller. The output D_{pi} of the S-R flip flop current regulator containing a small amount of variations provides the correction to the final duty ratio. On the other hand, output voltage V_o control is achieved by forward converter. Figure 8 shows a Fuzzy voltage controller with a open loop duty ratio $D_{open,h}$ which is calculated similarly to $D_{open,p}$ in terms of power ratings of each converter

$$D_{open,p} = \frac{nV_o P_{p.pu}}{v_{dr} + nV_o P_{p.pu}}. \qquad (27)$$

Final duty ratio D_p is obtained by adding the duty ratio D_{pi} from controller with $D_{open,p}$. The output voltage control response is much faster than single stage scheme since two converters are employed for separate control function.
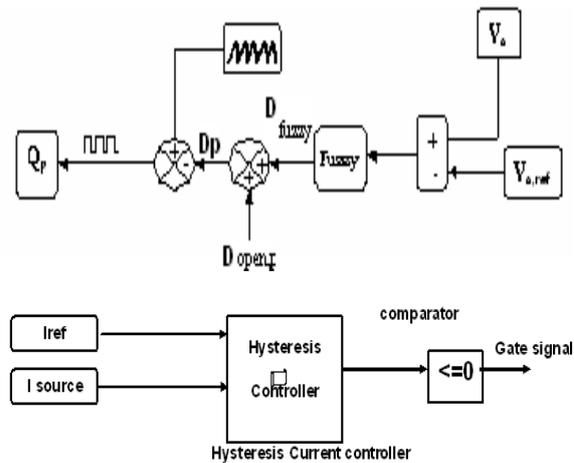
Fig. 6: Converter controllers.

5. Design Example

The proposed PFC circuit is designed according to the following parameters:

- total output power (P_o) = 200 [W],
- input voltage (V_s) = 230 [V],
- output voltage (V_o) = 48 [V],
- line frequency = 50 [Hz],
- switching frequency = 37000 [Hz],
- output dc capacitance (C_o) = 1500 [μF],
- transformer turns ratio (n) = 4,41:1.

  Forward Converter:

- power rating = 109,4 [W],
- magnetizing inductance (L_{mp}) = 0,5 [mH],

- DC capacitance = 660 [μF].

Flyback Converter:

- power rating = 90,6 [W],

- magnetizing inductance (L_{mh}) = 1,2 [mH].

The proposed scheme provides small input inductor since the inductor current depends on, dc-link voltage is smaller so that the voltage stress on the switch of the forward converter is less, the power rating of DC/DC stage is a bit higher than average power due to lower harmonic components, and the diode reverse recovery loss is minimized because of the tailed diode conduction mode.

The membership functions of the inputs error, change in error and output are triangular as shown in Fig. 7.
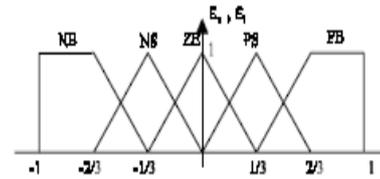
Fig. 7: Single stage PFC.

Tab.1: FIS rule table.

E/ce	NB	NS	ZE	PS	PB
PB	NS	NS	NS	NS	NB
PS	ZE	ZE	ZE	NS	NS
ZE	ZE	ZE	ZE	ZE	ZE
NS	PS	PS	ZE	ZE	ZE
NB	PB	PS	PS	PS	PS

Inference system rule table used for the design of fuzzy controller is shown in Fig. 8.
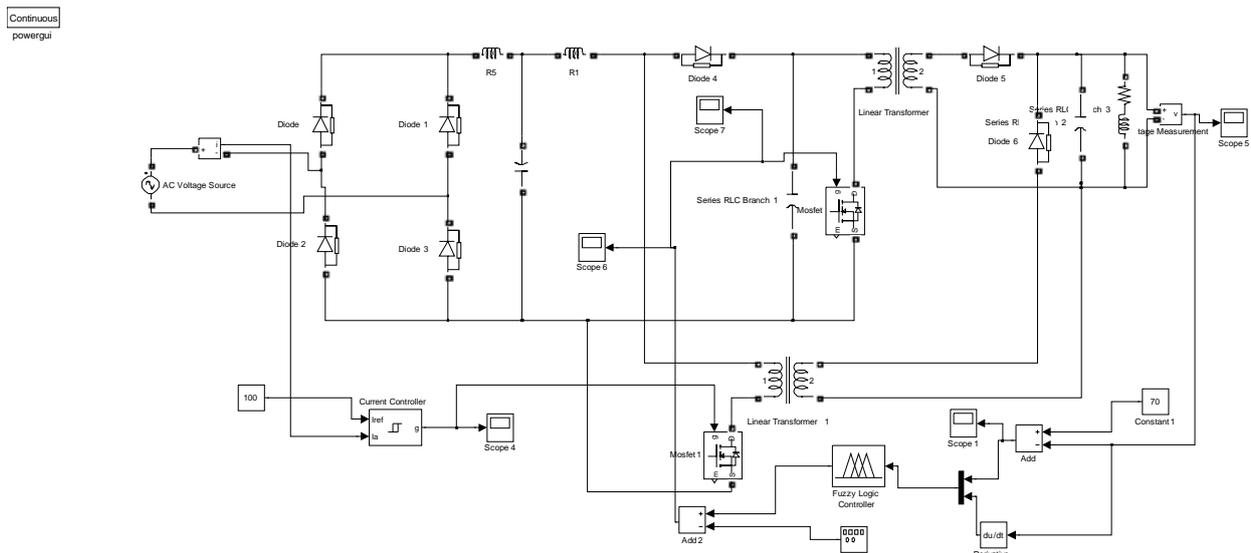
Fig. 8: MATLAB/Simulink model of proposed topology.

6. Simulation and Results

The proposed topology is implemented using MATLAB/Simulink is shown in Fig. 8. The results of the proposed topology are shown in Fig. 9, 10 and 11. Unity power factor and tight output voltage (48 V) regulation can be achieved. The dc-link voltage is 1,414*Vs=325 V, and the voltage ripple of the dc-link is 0,4 V which mainly depends on the dc-link capacitance. Two control systems are implemented to prove the proposed scheme

7. Conclusion

A parallel-connected single phase power factor correction (PFC) topology using Fuzzy controller for forward converter and a flyback converter has been proposed. It has been shown that output voltage regulation is achieved by DC/DC cell and the input power factor correction is achieved by AC/DC PFC cell. The proposed approach offers the following advantages: smaller size passive components, lower voltage-ampere rating of DC/DC stage, and higher efficiency. Simulation results demonstrate the capability of the proposed scheme.
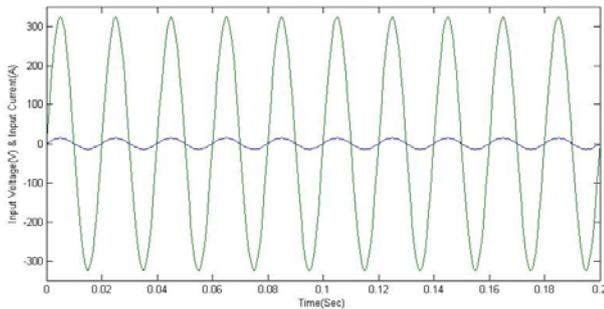
Fig. 9: Source voltage & current.
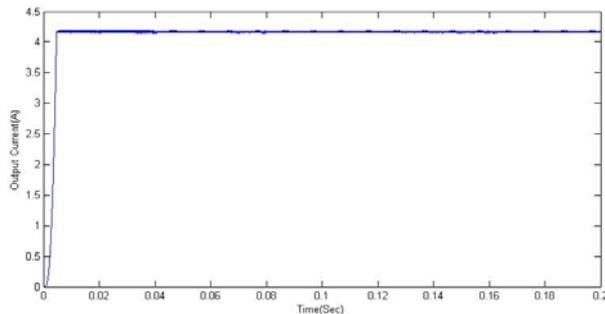
Fig. 10: Output current.
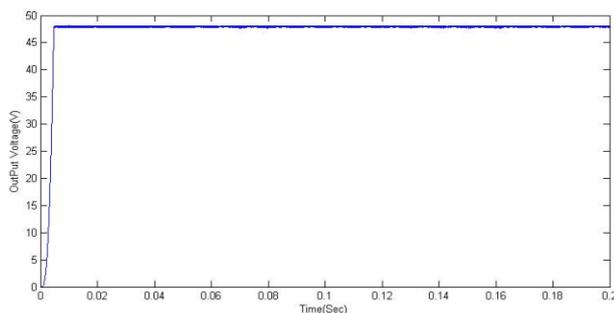
Fig. 11: Output voltage.

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