

# COMPACT AND ENERGY EFFICIENT QCA BASED HAMMING ENCODER FOR ERROR DETECTION AND CORRECTION

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**Abstract.** Quantum-dot Cellular Automata (QCA) are preferred for realizing logic circuits at nanoscale dimensions along with a high level of integration and minimal energy consumption. Hamming code is a set of entropy codes used for error detection and correction in communication systems. Error detection and correction is carried out with the help of parity bits which are appended with the original bits. Designing a Hamming encoder in nanoscale has its own merits such as optimized area, reduced energy dissipation and lower QCA cost. This work proposes two QCA-based (7, 4) Hamming encoder designs; multilayer (proposed-1) and coplanar (proposed-2) structure with area and energy analysis. Proposed-1 encoder has achieved reduction of cell area by 12.5 %, 34.58 % in terms of cell count, and reduction in total energy dissipation of 26.8 % when compared to reference encoder. Proposed-2 encoder has achieved reduction of 18.75 % in area, 44.15 % in terms of cell count, and 16.5 % in total energy dissipation when compared to reference encoder. In terms of QCA cost, reduction of 12.5 % is achieved in case of proposed structures. The energy dissipated in the proposed designs is less compared to reference encoder. Proposed-2 structure is more efficient compared to multilayer and reference encoder in terms of cell count, cell area and QCA cost. The QCA circuits are realized in QCADesigner and analyzed energy in QCADesigner-E.

## Keywords

**Clocking, coplanar, energy dissipation, Hamming encoder, multilayer, QCA.**

## 1. Introduction

A replacement for the widely used CMOS technology is required since it is reaching its physical limits. One of the best substitutes for CMOS technology is Quantum-dot Cellular Automata (QCA). The difficult factors for nano-computer and nano-communication devices include device density, operation speed and power loss. Effective area utilization at the nanoscale is a barrier to building high power consumption architecture in CMOS [1]. A nanoscale technology noted for its low energy power dissipation, rapid switching times, high operating frequencies, and compact size QCA. At the nanoscale, it is utilized to create combinational and sequential logic circuits.

Gallium Arsenide is one of the semiconductors used to make quantum dots. The columbic force of attraction between the QCA cells causes self-production in cellular automata. High switching speed, small device size, and extremely low power consumption are all features of QCA [2]. Here, electrons play a crucial part in both the transmission of digital information and numerous logic operations.

QCA circuits offer many benefits, including device shrinkage with faster switching times, and lower energy/ power consumption. Information can be processed faster in QCA design, which also reduces energy dissipation at the nanoscale. Contrary to conventional CMOS technology, QCA mandates the use of a clock for both combinational and sequential circuits. The quantum dots are a crucial part of the QCA. It is a three-dimensional structure that holds an electron, i.e., electrical charge. QCA decreases the data processing latency, increasing operation speed and frequency [3]. A QCA cell, Majority Voter

(MV) gate and inverter, and a simulation type setup make up the device. For the purpose of building digital logic circuits with higher integration and low energy consumption, QCA is a promising alternative to CMOS technology.

The data provided during digital transmission may be distorted by noise and other environmental conditions. In the event of any transmission error, data loss happens. An error happens when the input data and the transmitted data do not agree. Important data is lost as a result of the error. Data is conveyed as bits, or '0' and '1'. The performance of the entire system could be affected by any change to one of the bits. When the bit '0' is changed to the bit '1' or vice versa, bit errors happen [1].

Hamming codes or linear block codes are the set of codes which perform error detection and correction by adding parity bits thereby giving rise to an effective error correction coding system. Basically, in Hamming communication network, redundancy bits are added for error detection and correction. The actual message data and parity bits are transmitted in coded format over the channel. When the receiver gets the coded signal, it separates the parity bits from the message bit and if the error is detected, it is further corrected. A (7, 4) Hamming encoder encodes 4 bits of data into 7 bits by including three parity bits [4].

The work proposes two optimized (7, 4) Hamming encoder designs. The objective of this proposed work is to minimize the cell count, cell area, QCA cost and energy dissipation by realizing different configurations of (7, 4) Hamming encoder. Hamming encoder is realized in both coplanar and multilayer structures. All the structures are implemented and simulated using QCADesigner 2.0.3 and analyzed energy using QCADesigner-E.

The paper is divided into different sections. The literature review was carried out on different papers and relevant topics in Sec. 2. The basic QCA technology, design and implementation of the proposed (7, 4) Hamming encoder is written in Sec. 3. and Sec. 4., respectively. The results of the implementation are discussed in Sec. 5. The conclusions derived are discussed in Sec. 6.

## 2. Literature Review

Quantum dot Cellular Automata (QCA) is a new computing paradigm that relies on quantum-mechanical effects to perform logic operations. It is a promising technology that has the potential to revolutionize computing by providing high-speed, low-power, and high-density devices.

Single-bit errors can be found if the parity count inverts the number of ones is not the same. A data bit may be flipped by noise during transmission. By adding codes with a greater number of parity bits, it is possible to find two-bit faults, each of which is calculated on a unique combination of bits in the data [4].

Forward Error Correction (FEC), which is used in data transmission, refers to a receiver's capacity to fix faults in the data it receives. A transmitting station must amplify the transmitted data in order to make this possible. By using a block parity technique, Hamming codes reduce the cost of implementing forward error correction. FEC can be implemented using various codes, such as Hamming codes, Reed-Solomon codes, and convolutional codes. Each code has its own characteristics and advantages, and the choice of code depends on the specific requirements of the communication system [5].

QCA clocks are used to regulate and synchronize the information flow. Additionally, it supplies the circuit with power. The four clock phases that each cell in a QCA has are Switch, Hold, Release, and Relax. The barriers are raised during the first phase (the switch phase), which results in an increase in the forces opposing the passage of electrons inside each cell while the movement of electrons gradually declines inside the cell [6].

In QCA, each cell contains four quantum dots. Two free electrons that are positioned diagonally across from one another charge each cell. The electrons are compelled to occupy the corner-most location of the cell as a result of tunnelling between adjacent dots caused by mutual electrostatic forces (repulsion). Additionally, the QCA cell has its own dimensions, which are highly important when calculating area. These cells have a height and breadth of 18 nm and 2 nm, respectively, which separates each one from its neighbor [8].

In the Hamming code generator, superfluous bits are used to encrypt message bits. The extra bits positioned at various locations in the message bits are known as parity or redundant bits. The receiver receives the coder bits, does a recalculation to acquire the error bits, and then completes the required calculation. The Hamming encoder works by adding extra bits, called parity bits, to a message based on its original bits. The parity bits are calculated in a way that allows the receiver to detect and correct any single-bit errors that may occur during transmission. The number of parity bits added depends on the number of data bits being encoded and the level of error correction required [9].

In QCA, the state of the quantum dots represents the bits of the encoded message. To detect a single-bit error in a Hamming encoded message using QCA, we can use a majority function, which is a basic building block of QCA circuits. A majority function accepts

three inputs and output will be the majority value of those inputs [10].

In QCA, the clocking is achieved by applying a periodic voltage signal to the cells of the array. This voltage signal causes the electron charge in the quantum dots to oscillate, which in turn causes the cells to transition between different states. By carefully controlling the timing and amplitude of the clock signal, the QCA array can be made to perform logic operations with high precision and efficiency [13].

Hamming code uses the parity bits, similarly to other error detection and correction codes. These bits are added to data in order to verify its accuracy when it is read or received during a data transmission. An error-correction code can pinpoint the position of a single bit defect within a data unit by using multiple parity bits.

### 3. Basics of QCA

#### 3.1. QCA Cell

The most elemental component of QCA is the QCA cell. Each QCA cell contains four quantum dots, and each of them represents an electron in motion. The holes are comparable to the dots in the QCA cell if the electron is like the electron in an atom in a cell [12]. Additionally, the QCA cell has its own dimensions, which are highly important when calculating area. Each QCA cell is 2 nm apart from its neighboring cell and measures 18 nm in height and breadth. Each of two polarizations indicates one of the two configurations:  $P = +1$  denotes logic high, while  $P = -1$  denotes logic low as shown in Fig. 1.

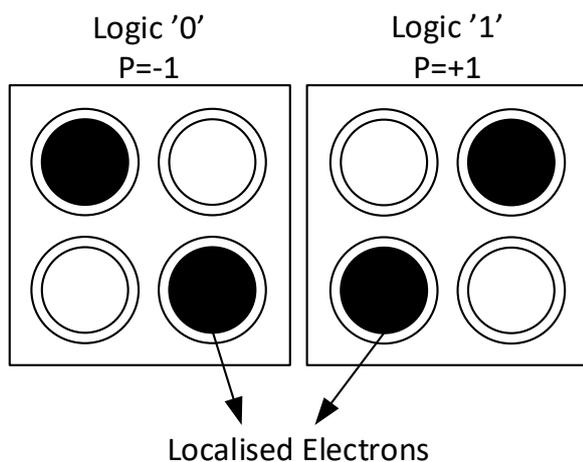


Fig. 1: QCA cell with polarity '+1' and '-1'.

**QCA Wire:** The simplest arrangement that is possible in QCA is by arranging the quantum dot cells in series. If there is change in polarization in any of the

four cells, the remaining four cells immediately synchronize to the polarization of other cells by columbic interaction between them [11].

The MV gate and inverter are the foundation of QCA. In the QCA logic, the MV gate is the common gate. By switching the polarity of one input to +1 or -1, it can be made into an AND or OR gate. Three input cells, one voter cell, and one output cell make up the MV gate [10]. When creating digital circuits with QCA and other digital building blocks like exclusive OR gates, the inverter gate is crucial. The inverter complements the input.

#### 3.2. QCA Clocking

A clock is required by every QCA circuit in order to synchronize and regulate the information flow. It gives the circuit the power it needs to function. The QCA clock consists of four phases. There is a  $90^\circ$  lag between neighboring phases [11]. The potential barriers that impact a cluster of QCA cells or the clocking zone are still elevated or lowered, the clock changes phase. The clocking system is demonstrated using the QCA binary wire [4]. Sub-array 1 is initially swapped in accordance with the input fixed. Sub-array 2 then begins to switch while sub-array 1 moves into the hold phase. Since sub-array 3 is in a relaxed state, it will not affect sub-array 2's computational state. Sub-array 1 releases a phase at the following phase, while sub-array 2 is in a hold state and supplies sub-array 3 with input. Information is transferred in a pipeline fashion with a  $90^\circ$  phase change from one clock zone to another [7].

#### 3.3. Simulation Engine and Setup

In QCA, there are two techniques to design circuits: using a coherence vector with energy or a bi-stable approximation. In QCADesigner-E, coherence vectors with energy are created. When compared to the coherence vector, the Bi-stable approximation is the fastest since it simulates the circuit without time dependencies. The coherence vector with energy approximation, however, depends on time [14]. The energy dissipation measurements and calculations are more accurate when using a vector. When compared to bi-stable approximation, it is slower. Two forms of simulation type setup support the simulation engine: exhaustive and vector table [13].

The vector table is preferred for larger circuits because all potential scenarios must be tested. The tabulated data of different engine setups refers to [15]. In QCA circuits, the QCA cell sizes are also important. The QCA cell's height and breadth are both 18 nm, and its dot's diameter is 5 nm. Each QCA cell is 2 nm apart from its neighboring cell. Layer separation is 11.5 nm,

and radius of effect is 65 nm. Circuits can be built in QCA in two different ways: as single-layer structures or as multilayer structures.

### 3.4. Crossover and Multilayer Design

QCA has two types of crossovers namely, multilayer and coplanar. Single-layer designs are feasibly done using coplanar crossover approach. For coplanar crossings, two cell types are required (regular and rotated). Rotated cells can be utilized for coplanar wire crossing because, when properly aligned, the regular cell and the rotated cell do not interact with each other. Similar to the many metal layers in a standard circuit, multilayer crossovers employ multiple layers of cells. Multilayer crossover is simpler to construct and has a reliable signal connection.

## 4. Implementation of (7, 4) Hamming Encoders

For effective communication, faults can be detected and corrected using error detection and correction techniques. The method of error detection is used to identify errors that are sent from the transmitter to the receiver. The process of rectifying data that has been transferred from transmitter to receiver is known as error correction. To find and fix faults, a Hamming code circuit is used. A systematic error detection and correction coding system is created by Hamming codes, which do both error detection and correction. Redundancies are essentially employed in these error-correcting codes for the purpose of error identification and correction. When the data is read or received, parity bits are added to it in order to verify its accuracy. An error detection-correction code may locate the data unit as well as detect a single-bit error in the data unit by using more than one parity bit. When data is received by the receiver, the parity bits and the real message are separated. If there are any problems, they are found and fixed. Parity bits and the actual message are transferred together over the channel.

The realization of the (7, 4) Hamming encoder is inspected in QCA using the top-down approach. The block diagram of the (7, 4) Hamming encoder is shown in Fig. 2. Proposed designs consist of three 3-input exclusive OR gates. In Fig. 2, I6, I5, I4, I3 represent inputs and E6, E5, E4, E3, E2, E1, E0 represent outputs. In (7, 4) Hamming encoder, the first four output bits E6, E5, E4, E3 can be directly obtained from the information bits. The next three supervision bits are obtained by conducting exclusive OR operation of the bits as shown in Eq. (1), Eq. (2) and Eq. (3)

which implies that three 3-input exclusive OR gates are required, and circuit architecture of the encoder is as illustrated in Fig. 2.

$$E2 = I6 \oplus I5 \oplus I4, \tag{1}$$

$$E1 = I6 \oplus I5 \oplus I3, \tag{2}$$

$$E0 = I6 \oplus I4 \oplus I3. \tag{3}$$

The QCA circuits of the proposed-1 (7, 4) Hamming encoder and proposed-2 (7, 4) Hamming encoder using QCADesigner are shown in Fig. 3 and Fig. 4, respectively. From the QCA designs, it is analyzed that proposed-1 multilayer (7, 4) Hamming encoder occupies an area of  $0.16 \mu^2$  and requires 123 cells, whereas proposed-2 coplanar (7, 4) Hamming encoder design requires an area of  $0.13 \mu^2$  and can be realized using 105 cells, which is less compared to design in [4].

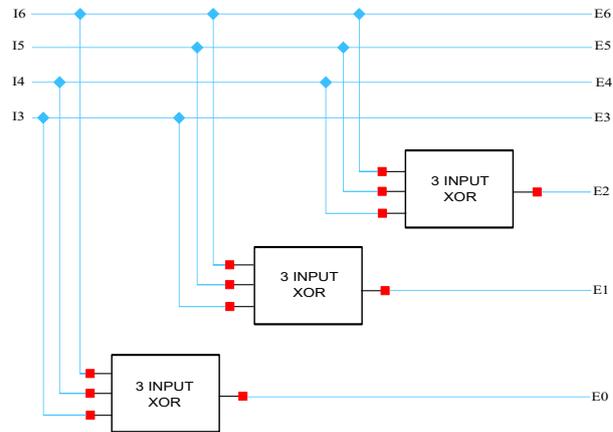


Fig. 2: Block diagram of (7, 4) Hamming encoder circuit.

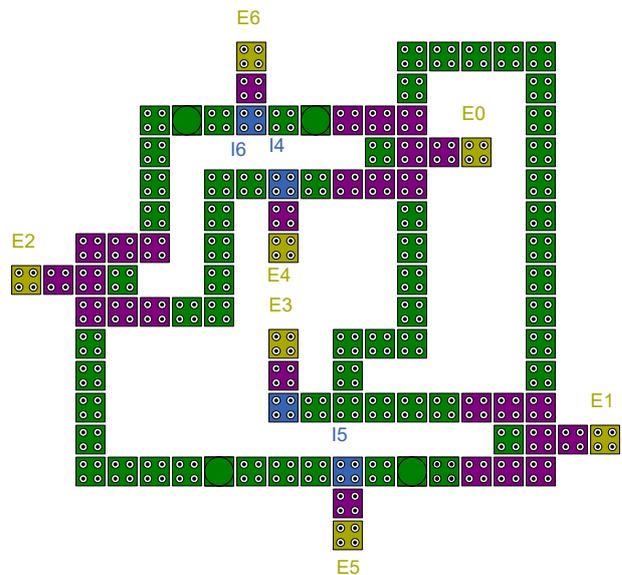


Fig. 3: Proposed-1 multilayer (7, 4) Hamming encoder circuit.

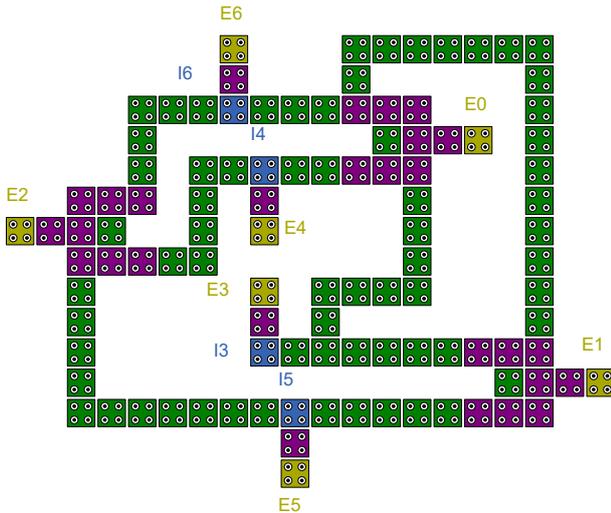


Fig. 4: Proposed-2 coplanar (7, 4) Hamming encoder circuit.

The Hamming encoder in [4] follows multilayer crossover structure which requires higher cell count and cell area. With the increase in area, the QCA cost will also increase. The proposed-2 coplanar design overcomes these drawbacks by using simple gates with reduced number of cells and less area usage. The exclusive OR gates are replaced with cells which require less area. The proposed-2 coplanar design consists of three exclusive OR gates with 11 cells whereas the reference circuit [4] consists of exclusive OR gates with 14 cells. The circuit has reduced area with a smaller number of cells. From Eq. (1), Eq. (2) and Eq. (3), combination of inputs is considered to obtain exclusive OR outputs.

### 5. Results and Discussions

The results of Hamming encoders are discussed in this section. The simulation results of Hamming encoder are shown in Fig. 5 and the values obtained (cell count, cell area, and energy dissipation) are tabulated in Tab. 1 and Tab. 2, respectively. The input signals named as I6, I5, I4, I3 are represented in blue font color and the output signals labeled as E1, E2, E3, E4, E5, and E6 are represented in yellow font color. It is clear that the outputs E6, E5, E4, and E3 agree with the input, while E2, E1, and E0 are obtained in accordance with the supervision relationship, demonstrating that the encoder has successfully carried out the intended function using Eq. (1), Eq. (2) and Eq. (3). It is observed that the proposed structures has an effective area utilization of 12.5 % in case of proposed-1 and 18.75 % in case of proposed-2 which is more effective compared to [4]. The total cell count is reduced by 34.57 % in case of proposed-1 and 44.15 % in case of proposed-2 compared to [4]. The total cell area is the product of the number of cells and the single cell

dimension. The encoder designed in [4] requires a more number of cells and hence total cell area increases. The proposed-2 circuit overcomes this limitation by using coplanar structure.

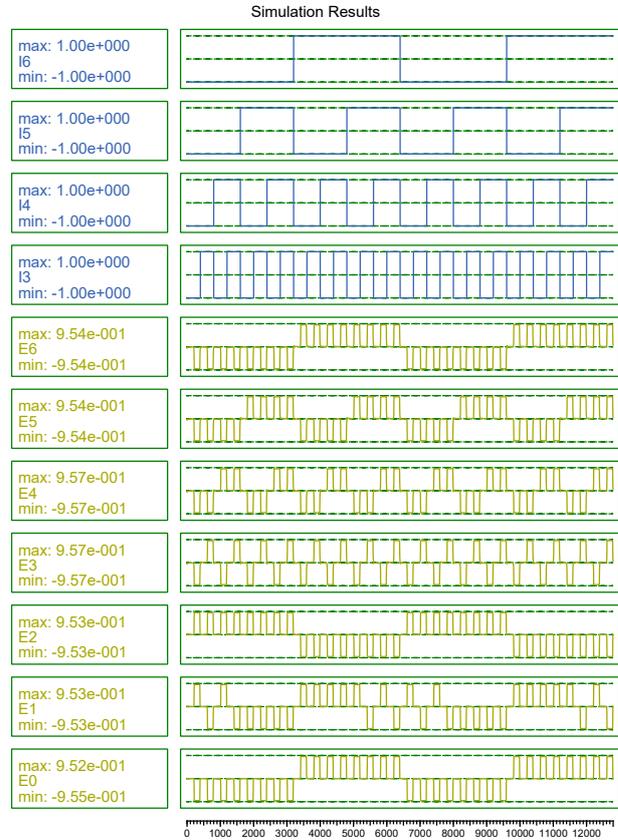


Fig. 5: Simulation results of (7, 4) Hamming encoder.

Tab. 1: Comparison of (7, 4) Hamming encoders.

QCA Parameters	[4]	Proposed-1 (multilayer)	Proposed-2 (coplanar)
Cell count	188	123	105
Total area ( $\mu\text{m}^2$ )	0.16	0.14	0.13
Cell area ( $\text{nm}^2$ )	60912	39852	34020
Latency	0.5	0.5	0.5
Cost	0.04	0.035	0.0325

QCA cost function is a product of latency and cell area. The cost function turned out to be 0.035 for proposed-1 multilayer encoder circuit and 0.0325 for proposed-2 coplanar encoder circuit. From Tab. 1, it can be inferred that the QCA cost function has drastically reduced when compared to circuit in [4] which makes the proposed design highly optimized.

The energy dissipation values of (7, 4) Hamming encoders obtained is as listed in Tab. 2. The total energy dissipation of proposed-1 circuit turned out to be  $5.51 \cdot 10^{-2}$  eV. It can be analyzed that the proposed-1 multilayer Hamming encoder has less energy dissipation compared to the one proposed in [4], i.e., reduction of 26.34 % is achieved. For proposed-2 coplanar

(7, 4) Hamming encoder, energy analysis turned out to be  $6.23 \cdot 10^{-2}$  eV and reduction in energy dissipation of 16.84 % was observed.

**Tab. 2:** Energy analysis of (7, 4) Hamming encoders.

Energy Analysis	[4]	Proposed-1 (multilayer)	Proposed-2 (coplanar)
Average energy dissipation (meV)	6.8	5.01	5.65
Total energy dissipation (meV)	74.8	55.1	62.2

The proposed Hamming encoder designs are both cost and area effective and dissipates lesser energy when compared to circuit in [4]. During the energy analysis, it is observed that proposed-1 design has lesser energy dissipation when compared to Hamming encoder in [4] and proposed-2 design. Trade-offs can be made in terms of cell area and energy dissipation.

## 6. Conclusion and Future Research

The proposed work illustrates the realization of compact (7, 4) Hamming encoders. CAD tools, QCADEsigner and QCADesigner-E are used for realizing the circuits and for energy analysis. The QCADesigner is used to realize the circuits and to measure the circuit parameters including cell count, cell area, latency, QCA cost and clock zone. QCADesigner-E is used to determine total and average energy dissipation. Proposed-1 (7, 4) Hamming encoder has achieved an improvement of 12.5 % in cell area and 34.57 % in cell count compared to [4]. Proposed-2 (7, 4) Hamming encoder has achieved 18.75 % reduction in area, 44.15 % reduction in cell count, and 12.5 % reduction in cost in comparison to the [4]. Proposed -1 circuit has a reduction of 26.4 % in average energy dissipation and proposed-2 circuit has achieved a reduction of 16.77 %. Proposed-2 circuit is more efficient compared to multilayer structure in terms of cell count, cell area, and QCA cost. The optimization of the (7, 4) Hamming encoder can be done using multilayer concepts which will further yield better results. The proposed design can be used for the implementation of Hamming decoder and Hamming communication network in addition using proposed (7, 4) design, optimized (15, 11) structures can be realized.

## Author Contributions

B.S.P conceptualized the idea, methodology, design, and analysis. Review of literature, design methodology and implementation were contributed by M.P. and

N.K. All authors contributed to the analysis of the design and results and provided inputs to the manuscript. All authors were involved in drafting the paper from the initial stages, editing, and revising the same.

## References

- [1] HARSHITHA, S., T.N. DHANUSH and B.S. PREMANANDA. A Novel QCA based Compact Scan Flip-flop for Digital Design Testing. *International Journal of Engineering and Advanced Technology (IJEAT)*. 2019, vol. 9, iss. 1, pp. 6681–6686. ISSN 2249-8958. DOI: 10.35940/ijeat.A1973.109119.
- [2] AMLANI, I., A. O. ORLOV, G. TOTH, G. H. BERNSTEIN, C. S. LENT and G. L. SNIDER. Digital Logic Gate Using Quantum-Dot Cellular Automata. *Science*. 1999, vol. 284, iss. 5412, pp. 289-291. ISSN 0036-8075. DOI: 10.1126/science.284.5412.289.
- [3] KHAN, A. and R. CHAKRABARTY. Design of Ring and Johnson Counter in a Single Reconfigurable Logic Circuit in QCA. *International Journal of Computer Science and Technology*. 2013, vol. 4, iss. 1, pp. 363–367. ISSN 0976-8491.
- [4] HUANG, J., G. XIE, R. KUANG and F. DENG. QCA-based Hamming code circuit for nano communication network. *Microprocessors and Microsystems*. 2021, vol. 84, iss. 1, pp. 1–8. ISSN 1872-9436. DOI: 10.1016/j.micpro.2021.104237.
- [5] HAMDOON, A. M. A., Z. G. MOHAMMED and E. A. MOHAMMED. Design and implementation of single bit error correction linear block code system based on FPGA. *Telkomnika (Telecommunication Computing Electronics and Control)*. 2019, vol. 17, iss. 4, pp. 1785–1795. ISSN 2302-9293. DOI: 10.12928/TELKOMNIKA.v17i4.12033.
- [6] DHANUSH, T. N., S. HARSHITHA and B. S.PREMANANDA. Introducing Galois field polynomial addition in quantum-dot cellular automata. In: *2020 International Conference on Advances in Computing, Communication & Materials (ICACCM)*. Dehradun: IEEE, 2020. pp. 282–288. ISBN 978-1-7281-9785-2. DOI: 10.1007/s13204-019-01045-x.
- [7] MUKHERJEE, C., S. PANDA, A. K. MUKHOPADHYAY and B. MAJI. Introducing Galois Field Polynomial Addition in Quantum-Dot Cellular Automata. *Applied Nanoscience*. 2019, vol. 9, iss. 1, pp. 2127–2146.

- ISSN 2190-5517. DOI: 10.1007/s13204-019-01045-x.
- [8] PREMANANDA, B. S., SOUNDARYA S. and CHAITRA D. K. S. Compact QCA based JK Flip-Flop for Digital System. *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*. 2019, vol. 8, iss. 12, pp. 3182–3185. ISSN 2278-3075. DOI: 10.35940/ijitee.L3074.1081219.
- [9] SUCHARITHA, D., R. N. PRUDHVI, R. B. SRAVYA and R. V. SUDHEER. GDI Logic Based Design of Hamming-Code Encoder and Decoder for Error Free Data Communication. In: *2019 3rd International Conference on Computing Methodologies and Communication (ICCMC)*. Erode: IEEE, 2019. pp. 1–5. ISBN 978-1-5386-7808-4. DOI: 10.1109/ICCMC.2019.8819665.
- [10] PREMANANDA, B. S. and T. N. DHANUSH. Design and Analysis of QCA based Area Efficient 4x8 SRAM array. In: *2020 International Conference on Advances in Computing, Communication & Materials (ICACCM)*. Dehradun: IEEE, 2021. pp. 283–288. ISBN 978-1-7281-9785-2. DOI: 10.1109/ICACCM50413.2020.9399208.
- [11] ASKARI, M. and M. TAGIZAHDEH. Logic Circuit Design in Nano-Scale using Quantum-Dot Cellular Automata. *European Journal of Scientific Research*. 2011, vol. 48, iss. 3, pp. 516–526. ISSN 1450-216X.
- [12] SAFOEV, N., G. ABDUKHALIL and K. A. ABDISALOMOVICH. QCA based Priority Encoder using Toffoli gate. In: *2020 IEEE 14th International Conference on Application of Information and Communication Technologies (AICT)*. Tashkent: IEEE, 2020. pp. 1–4. ISBN 978-1-7281-7386-3. DOI: 10.1109/AICT50176.2020.9368637.
- [13] CHEN, P., Y. WANG., Q. YU, Y. FAN and R. FENG. Hamming Distance Encoding Multi-hop Relation Knowledge Graph Completion. *IEEE Access*. 2020, vol.8, iss. 1, pp. 117146–117158. ISSN 2169-3536. DOI: 10.1109/ACCESS.2020.3004448.
- [14] PREMANANDA, B. S., U. K. BHARGAV and K. S. VINEETH. Compact Qca Based Serial-Parallel Multiplier For Signal Processing Applications. *International Journal of Scientific and Technology Research*. 2020, vol. 9, iss. 3, pp. 31–38. ISSN 2277-8616.
- [15] PREMANANDA, B. S., S. H. MANALOGOLI and K. J. NIKHIL. Area and Energy Optimized QCA Based Shuffle-Exchange Network with Multicast and Broadcast Configuration. *Advances in Electrical and Electronics Engineering*. 2021, vol. 19, iss. 4, pp. 322–332. ISSN 1804-3119. DOI: 10.15598/aece.v19i4.4280.
- [16] DAS, J. C., D. De, S. P. MONDAL, A. AHMADIAN, F. GHAEMI and N. SENU. QCA Based Error Detection Circuit for Nano Communication Network. *IEEE Access*. 2019, vol. 7, iss. 1, pp. 67355–67366. ISSN 2169-3536. DOI: 10.1109/ACCESS.2019.2918025.

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