main size calculated by method proposed by Langford for the (111) and (222) lines. It is seen from the comparison the values of domain size that the method proposed by Langford may be used only to comparison of the investigated samples.

| Table 3. Probability of stacking faults and the values of surface-weighted domain size. |
| Sample α | D_{X} [nm] | D_{Y} [nm] |
| 1 | 0.005 | 190 | 275 |
| 2 | 0.007 | 225 | 480 |

In the Table 3 is presented the probability of stacking faults in samples 1 and 2. Influence the stacking faults on the values of surface-weighted domain size is apparent from Table 3. The correction on stacking faults for the values of surface-weighted domain size was calculated according to formula

\[ \frac{1}{D_{\text{eff}}} = \frac{1}{D_{b}} + \frac{1.5 \alpha}{\sqrt{\sum_{i} b \cdot k + b \cdot f}} \]

posed by [6]. The values of surface-weighted domain size after correction are presented in Table 3 too.

The lattice strain was calculated without and with the correction on the stacking faults. Wern at all [7] proposed for the thin films the elastic constant \( S_{2} \) calculate by constraint Voigt model

\[ S_{2} = \frac{\gamma S - 2 \gamma S_{44}}{3(2\alpha + 1 - \gamma^2)} \]

where \( S = 4\alpha S_{44} + 2h \cdot k_{1} + 2h \cdot k_{2} + k_{1} \cdot k_{2} + k_{1} \cdot k_{3} + k_{2} \cdot k_{3} \)

\( \gamma = k_{1} \cdot k_{2} \cdot k_{3} \)

and \( \gamma = k_{1} \cdot k_{2} \cdot k_{3} \cdot k_{4} \)

The data for the calculation the \( S_{2} \) was used from [8]. The correction on stacking faults was calculated in accordance with the formula (8). The calculated values of lattice strain are given in Table 4.

| Table 4. The values of lattice strain. |
| Sample | (\(\sigma_{1}, \sigma_{2}\)) without correction [MPa] | (\(\sigma_{1}, \sigma_{2}\)) after correction of stacking faults [MPa] |
| 1 (111) | 260 | 235 |
| (222) | 220 | 235 |
| 2 (111) | 250 | 215 |
| (222) | 190 | 215 |
| 3 (111) | 290 | - |

It is apparent from the Table 4 that the values of lattice strain after correction on the stacking faults are the same for the (111) and (222) lines.

5. CONCLUSIONS

The used method of approximation by Voigt function gives very good agreement between the experimentally measured diffraction lines and the calculated approximation functions.

The results of approximation are the parameters of the Voigt function which describe the physical profile of the broadening is it nothing any another deconvolution.

In the case that in the samples are present stacking faults it is necessary made the correction on the stacking faults as at calculation the values of domain size as at calculation of the lattice strain.

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1. INTRODUCTION

It is well known that Si surface pre-oxidation treatment and high quality thermal oxide preparation plays crucial role in unipolar technology. From that point of view, great attention has to be paid on the thermal SiO$_2$ growing with bulk and Si–SiO$_2$ interface densities of defects as low as possible. Due to downsizing of device dimensions the interface thickness also decreased thereby bulk defects are suppressed, however, one should mind in keep electrically active defects located at the Si–SiO$_2$ interface that can participate in electrically active defects. Moreover, electrical parameters of power device are partially influenced by defects in the substrate region of Si. Shrinkage of these defects is permanent task in high-quality substrate preparation and creation of defect-free region, so called cedube zone (D2Z). Capacitance methods are the most suitable diagnostics tool for investigation of such a defects and process optimisation as well.

In this work we characterised MOS capacitors (MOS-C) using \( C-V \) and \( I-V \) curves from which we evaluated free carriers concentration \( n(x) \), flat-band voltages \( \psi_{FB} \), effective defect charge \( Q_{D} \) and energy distribution of Si–SiO$_2$ interface trap density \( D_{it} \) respectively.

Electrically active defects in the substrate region were explored by measuring of generation lifetime \( \tau_{g} \) and surface generation velocity \( \psi_{s} \) using pulsed MOS-C-V technique, furthermore, depth profile of \( \psi(x) \) obtained using the time domain constant-capacitance technique (c-c-t) which is an modification of conventional C-T method [2]. Standard Deep Level Transient Spectroscopy (DLTS) have been also employed to our investigation. Breakdown voltage measurement and time-dependent breakdown were used for determination of SiO$_2$ layer electric strength [3].

2. EXPERIMENT

An n-type, phosphorus doped, \(<100>-oriented homogenous silicon wafer with resistivity 2-5 kΩ and thickness 300 μm was used as a substrate of the MOS-Cs. The gate SiO$_2$ layer was prepared by thermal oxidation in an atmosphere of dry oxygen at 1000°C. The thickness of the SiO$_2$ layer was about 40 and 28 nm. All gates were vapour deposited and patterned photolithographically. After manufacturing the MOS structures, the sample was annealed in N$_2 + H_2$ at 460°C for 20 minutes.

The measurements were performed on the MOS-Cs prepared by standard pre-oxidation treatment (BU5) and samples with intrinsic gettering by poly- 

Si deposition (DEP5). The MOS-Cs were characterized by capacitance and current methods. High frequency capacitance \( C-V \) and non-equilibrium capacitance-time \( C-V \) measurements were performed using the 4280 1 MHz C Meter/CV Plotter Hewlett-Packard [5]. Quasi-static \( C-V \) measurements were performed using the Keithley 595 Quasi-static C-V Meter. DLTS measurements were performed using the Polaron DLTS Spectrometer 4900. This spectrometer uses a boxcar detection system for acquiring the DLTS output signal. Breakdown measurements were performed using the Keithley 238 High Current Source Measure Unit.

3. RESULTS AND DISCUSSION

The flat-band voltage of MOS-C BU5 was calculated from \( V-C \) curve (Fig. 1) as \( V_{FB}=6.5 \) V, that indicates relatively high effective defect charge of \( N_{D}=2.6 \times 10^{13} \) cm$^{-2}$. C-V curve (Fig. 2) of
the sample BU3 reveals typical shape with long relaxation process duration (t=1500 s). However, there was no marked linear part in the Zerbst plot, therefore extracted lifetime is rather low, while surface velocity is at their typical value. It shows that thermal generation proceeds under non-constant generation rate. We suggest that increasing of generation rate (i.e. flow of minority carriers creating inversion layer under gate) is caused by traps located at the Si-SiO₂ interface.

Hence, we investigate Si-SiO₂ interface using quasi-static C-V measurement. Interface trap density determined at ±0.1 eV in the Si mid-gap was Dₜ=5.34×10¹² m⁻²eV⁻¹. According to energy distribution of Dₜ shown in Fig. 3, one can distinguish two deep levels near the mid-gap Eₜ₁ = Eₜ₂ = ±0.2 eV and Eₜ₃ = ±0.49 eV, which contribute to the enhanced carrier emission, thus generation minority carrier flux. Depth profile of generation lifetime was almost constant through depletion region with value equal to that obtained from Zerbst plot (τₐ=180 μs).

Three deep levels were finding from the DLTS measurement. These levels, also located near the mid-gap, originate from metal impurities of atoms Fe (Eₜ₁=±350 meV) and Au (Eₜ₂=±540 meV). Third level with activation enthalpy Eₜ₃=±530 meV was identified as Cu impurity and we associate this level to the Eₜ₃ obtained from energy distribution of Dₜ. The cross-section of all the traps was very low (n=5.5×10¹⁶ cm⁻³), consequently their electrical activity play insignificant role.

The measurement of breakdown voltages revealed typical process of drift current flow, which is given by SiO₂ quality and homogeneity. The value of breakdown voltage (V₉₀=40 V) does not change with lateral position on the wafer. We did not observe time dependent oxide breakdown.

According to C-V measurement of MOS-C DEF2 (Fig. 1) it can be seen that positive defect charge is lower according sample BU3 (Eₜ₃=0.2 V) to DEF2 (Eₜ₃=0.91 - 1.80 V), whereas C-V curve reveals usual shape. Here, steep increasing of capacitance, thus generation current appear at the earliest part of the relaxation process (up to 200 s). Since the Zerbst model could not be used for such a transient due to non-constant generation kinetics, we can explain the shape of observed C-V curve from depth profile of generation lifetime shown in Fig. 4. The C-V technique for depth profiling of generation lifetime measurement represents a modification of C-V method under constant depletion width maintaining by controlled voltage ramp. At the Fig. 4, Hold Time is the time interval between pulsing the MOS-C into deep depletion and applying controlled voltage ramp, hence, MOS-C followed C-V curve at this time interval. When the Hold Time is passed, capacitance is kept constant. Fig. 4 shows creation of DZ in Si depth (up to 3 μm), which is consistent with the earliest part of the C-V curve. Generation lifetime then increases toward surface but at approximately 2 μm it again decreases. However, from C-V measurement with Hold Times/300 s we find lifetime in order of ms in subsurface region (≈1 μm). So, it can be deduced that decline of generation lifetime at the beginning of depth profile is caused by surface generation while bulk is of high-quality.

In the other words, τₐ (s) measured with Hold Time=300 s is correct without influence of Si-SiO₂ interface trap emission. Our suggestion is supported with Dₓ(E) measurement where, again, two deep levels were identified which can act as efficient generation centres. Note that surface generation is time dependent during relaxation and can control this process if the lifetime is extremely high.

On the contrary, we connect decreasing of lifetime deeper in the bulk (3.5 μm) with presence of oxide precipitates.

Fig. 2. C-V curves of investigated structures with evaluated generation parameters.

Fig. 3. Energy distribution of interface trap density. Arrows label deep levels from the left side as Eₜ₁=0.49 eV and Eₜ₂=0.52 eV, respectively.

Fig. 4. Depth profile of generation lifetime of the sample DEF2 for Hold Time = 300 s (full circles) and 300 s (open circles). Dash line is drawn for eyes leading only.

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Fig. 5. Time-dependent breakdown of the sample DEF2

breakdown measurement reveals elevated conductance of insulator layer due to Poole-Frenkel emission. This effect was clearly demonstrated in the time-dependent breakdown measurement (Fig. 5) and on the plot of Im(E) versus E² (Fig. 6), which is commonly used to determine the dominant leakage current mechanism. The value of breakdown voltage was V₉₀=28 V.

Two deep levels were detected with activation enthalpies and capture cross-sections Eₜ₃=403 meV, Eₜ₄=571 meV and τₐ=2.0×10⁻²³ cm₃ s⁻¹, respectively from DLTS measurement. We assume that these levels originate from metal impurities of Ni (Eₜ₃=410 meV) a W (Eₜ₄=370 meV).

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Hence, we investigate Si-SiO₂ interface using quasi-static C-V measurement. Interface trap density determined at $\pm 1.1$ eV in the Si mid-gap was $D_{it}=5.34 \times 10^{13}$ m⁻²eV⁻¹. According to energy distribution of $D_{it}$ shown in Fig. 3, one can distinguish two deep levels near the mid-gap $E_{1} = 0.52$ eV and $E_{2} = 0.49$ eV, which can contribute to the enhanced carrier emission, thus generation minority carrier flux. Depth profile of generation lifetime was almost constant through depletion region with value equal to that obtained from Zerbst plot ($\tau=180$ µs).

Three deep levels were found from the DLTS measurement. These levels, also located near the mid-gap, originate from metal impurities of atoms Fe ($E_{1}=0.50$ meV) and Au ($E_{2}=0.52$ meV). Third level with activation enthalpy $E_{act}=530$ meV was identified as Cu impurity and we associate this level to the $E_{1}$ obtained from energy distribution of $D_{it}$. Cross-section of all the traps was very low ($\approx 0.5 \times 10^{15}$ cm⁻³), consequently their electrical activity play insignificant role.

The measurement of breakdown voltages revealed typical process of drift current flow, which is given by SiO₂ quality and homogeneity. The value of breakdown voltage ($V_{bd}=40$ V) does not change with lateral position on the wafer. We did not observe time dependent oxide breakdown.

Regarding to C-V measurement of MOS-C DEP2 (Fig. 1) it can be seen that positive defect charge is lower according to sample BU3 ($V_{pp} = 0.2$ V and $N_{pp}=0.91 - 1.81 \times 10^{13}$ cm⁻²), whereas C-V curve reveals unusual shape. Here, steep increasing of capacitance, thus generation current appear at the earliest part of the relaxation process (up to 200 s).

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Another deep levels were detected with activation enthalpies and capture cross-sections $E_{act}=403$ meV, $E_{act}=371$ meV and $E_{act}=8.1 \times 10^{13}$ cm⁻³, $E_{act}=2.5 \times 10^{13}$ cm⁻³, respectively from DLTS measurement. We assume that these levels originate from metal impurities of Ni ($E_{act}=10$ meV) a W ($E_{act}=370$ meV).

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