Silicon Resistivity Behaviour

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Abstract. *Intrinsic resistivity of any semiconductor silicon layer strongly depends on dopants and impurities concentrations. Structural properties, treating, coating, finishing etc. affect dynamic resistance behaviour of a given p-n junction in a wafer. It is important for massively used photovoltaics, optoelectronics, microelectronics, and other solid-state electronics. In this work, efficient, universally applicable methodology is presented to investigate silicon resistive parameters. First, the silicon band gap models are studied. Influence of electrical resistivity on resistances and complex impedance parts is investigated. Dynamic iterative numerical modelling and simulations combined with sparse-matrix experimental measurements lead to extrapolated behaviours of these resistive parameters. All parameters are investigated within acceptable practical interval up to extremals.*

Keywords

Electrical resistances, electrical resistivity, modelling and simulation, silicon wafer.

1. Introduction

Electrical characterization of any silicon-based structure relates to its pure-form diamond crystallization structure. Due to its temperature T dependent behaviour, a silicon doped layer bandgap voltage $E_g(T)$ at specified temperature T can be implicitly calculated from the $E_g(0)$ at reference temperature of $T(0) = 300$ K, as explained in references [1], [2], [3], [4], [5] and [6]. Hot purification and deposition processes, crystallization etc. influence random silicon granularity, consequently its resistivity, as depicted in [7], [8], [9] and [10]. The single-crystals and ultra-pure polycrystalline ingots at the impurity level under 10^{-9} % are used for semiconductor, microelectronic or optoelectronic production, while the rest at the impurity level up to 10^{-4} % is used for photovoltaics. The intrinsic electrons and holes equal concentrations $n = p$ of the highly pure silicon were estimated in [11] and [12] and, after some more experimental verifications, they were modified in [13] to widely accepted $n \approx 10^{10}$ cm^{-3} at reference temperature.

To obtain wafers with required electrical properties, monocrystalline, polycrystalline or amorphous silicon slices are intentionally surface-doped by Sb donor for p-type silicon and, P or B acceptors for n-type silicon, mostly. Radial dopant gradients and striations cause inhomogeneity of resistivity. SiO_2/SiO and CO/CO_2 impurities cause lower resistivity, under 50 Ω·cm at reference temperature. Monocrystalline resistivity expands up to 180 Ω·cm or even above 200 Ω·cm. Additional processes eliminate impurities thus the resistivity increases up to 4000 Ω·cm for high-ohmic applications, as mentioned in [1], [2], [3], [4], [5], [6], [7], [10] and [14]. The wettability of the resistivity strongly influences the morphology of synthesized nanowire arrays, too [15].

Electrical properties of silicon wafer cells are investigated via linear models, like in [16] and [17], based on single- or double-diode equivalent schematic diagrams. Silicon carriers' intrinsic mobility can be affected by several operational influences like temperature etc., so the structure of an optoelectronic telecommunications component might be limited in use, as mentioned in [18]. Besides, to detect structural defects, optical properties are widely tested in operation, as described in [1], [6], [7], [19], [20] and [21].

In this work, the external electrical parameters set of a specified polycrystalline silicon wafer cell is mea-

sured at preferred temperature interval and used to estimate intrinsic parameters relations and behaviour at common temperature interval up to extremals. Finally, complex impedance and frequency response are estimated within operational range for the specified silicon wafer.

2. Methodology, Simulation, Experiments and Results

In the first sub-section, silicon band gap behaviour is investigated using five common approaches. In the next sub-section, relationships and behaviour of intrinsic parameters based on resistivity are investigated. As the diode models are not practical for direct resistivity estimation due to final encapsulation of a silicon wafer cell, sparse data models and fast simulation of p-n junction internal properties are applied in this work. From the specified polycrystalline silicon wafer cell of the size $S = 20$ cm^2, external parameters like output voltage V_{out} up to open-circuit voltage $V_{OC} = 1.92$ V and output current I_{out} up to short circuit current $I_{SC} = 0.135$ mA are obtained by fast acquisition within temperature interval $T \in (273.15 \ldots 353.15)$ K. Maximum power point voltage $V_{MPP} = 1.32$ V and current $I_{MPP} = 0.1202$ mA are calculated. Based on such sparse matrix parameters, intrinsic parameters like dimensionless ideality factor n, series resistance R_s (Ω), shunt resistance R_{sh} (Ω), and complex impedance are obtained using iterative modelling and simulation. Finally, complex resistance parameters and frequency response are obtained for the specified wafer structure, based on previous resistances calculations.

2.1. Band Gap Behaviour

Based on approaches in [1], [2], [3], [4], [5] and [6], the band gap $E_g(T)$ simulated behaviour is obtained via equations Eq. (1), Eq. (2), Eq. (3), Eq. (4) and Eq. (5), at temperature interval $T \in (0 \ldots 450)$ K:

$$E_g(T) = E_g(0) - \frac{\alpha\Theta_p}{2}\left[\sqrt[p]{1+\left(\frac{2T}{\Theta_p}\right)^p} - 1\right] \quad (eV), \tag{1}$$

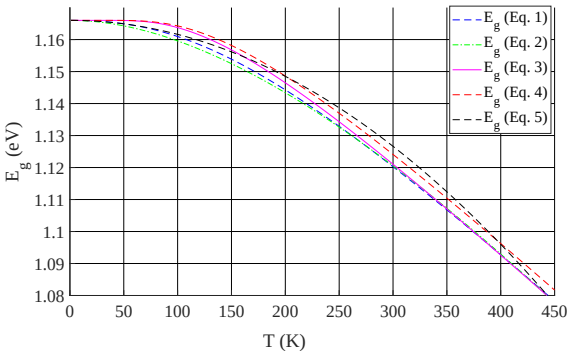
$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} = 1.166 - \frac{0.473T^2}{T+636} \quad (eV), \tag{2}$$

$$E_g(T) = E_g(0) - \frac{\alpha\Theta}{\exp\left(\frac{\Theta}{T}\right) - 1} \quad (eV), \tag{3}$$

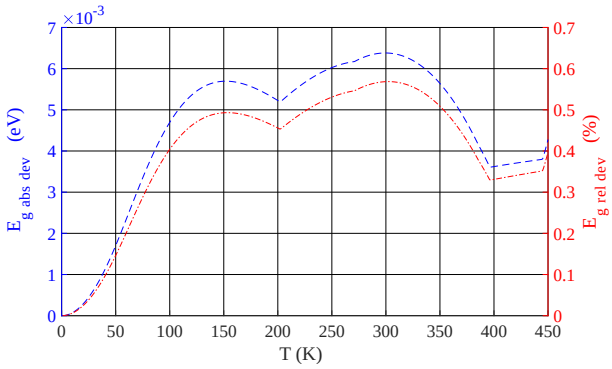
$$E_g(T) = E_g(0) - \frac{\alpha\Theta}{2}\left(\coth\left(\frac{\Theta}{2T}\right) - 1\right) \quad (eV), \tag{4}$$

$$E_g(T) = E_g(0) - \frac{\alpha\pi^2 T^2 \Delta^2}{3\Theta\left(1+\Delta^2\right)} \quad (eV), \tag{5}$$

where $\alpha = 0.473$, $\beta = 636$ are experimentally obtained material constants, $\Theta_p = 406$ or Θ are estimated or average phonon temperatures, while p and Δ are silicon material constant and phonon dispersion coefficient.



(a) $E_g(T) = f(T)$ behaviour.



(b) Absolute and relative deviations.

Fig. 1: Pure silicon intrinsic bandgap voltage.

Figure 1 shows the accuracy of the above five equations. Numerical results slightly vary with the simulated temperature interval, with the absolute deviation up to 0.00638 eV or relative deviation up to 0.5685 % among the highest and the lowest values of the equations set.

2.2. Intrinsic Parameters Relations and Behaviour

To investigate intrinsic parameters relations, the iterative model is stated by equations system Eq. (6), Eq. (7), Eq. (8) and Eq. (9):

$$n = \frac{q(B - V_{OC})}{k_B T \left\{ \ln\left(I_{SC} - \frac{V_{MPP}}{R_{sh}} - I_{MPP}\right) - \ln\left(I_{SC} - \frac{V_{OC}}{R_{sh}}\right) + \frac{I_{MPP}}{I_{SC} - \frac{V_{MPP}}{R_{sh}}} \right\}} \quad (-), \tag{6}$$

$$R_{sh} = \frac{(R_s I_{MPP} - V_{MPP}) \left[(B - V_{OC} - A)\, e^{\left(\frac{B}{A}\right)} + A e^{\left(\frac{V_{OC}}{A}\right)} \right]}{I_{MPP} \left[(V_{MPP} - R_s I_{MPP} + A)\, e^{\left(\frac{B}{A}\right)} - A e^{\left(\frac{V_{OC}}{A}\right)} \right]} \quad (\Omega), \tag{7}$$

$$R_s = \frac{V_{MPP}}{I_{MPP}} + \frac{A}{I_{MPP}} \left[1 + W\left(-e^{\left(\frac{V_{OC} - 2V_{MPP} - A}{A} \right)} \right) \right] \quad (\Omega), \tag{8}$$

$$r_s = \frac{R_s}{S} \frac{I_{MPP}}{V_{MPP}} \quad (-), \tag{9}$$

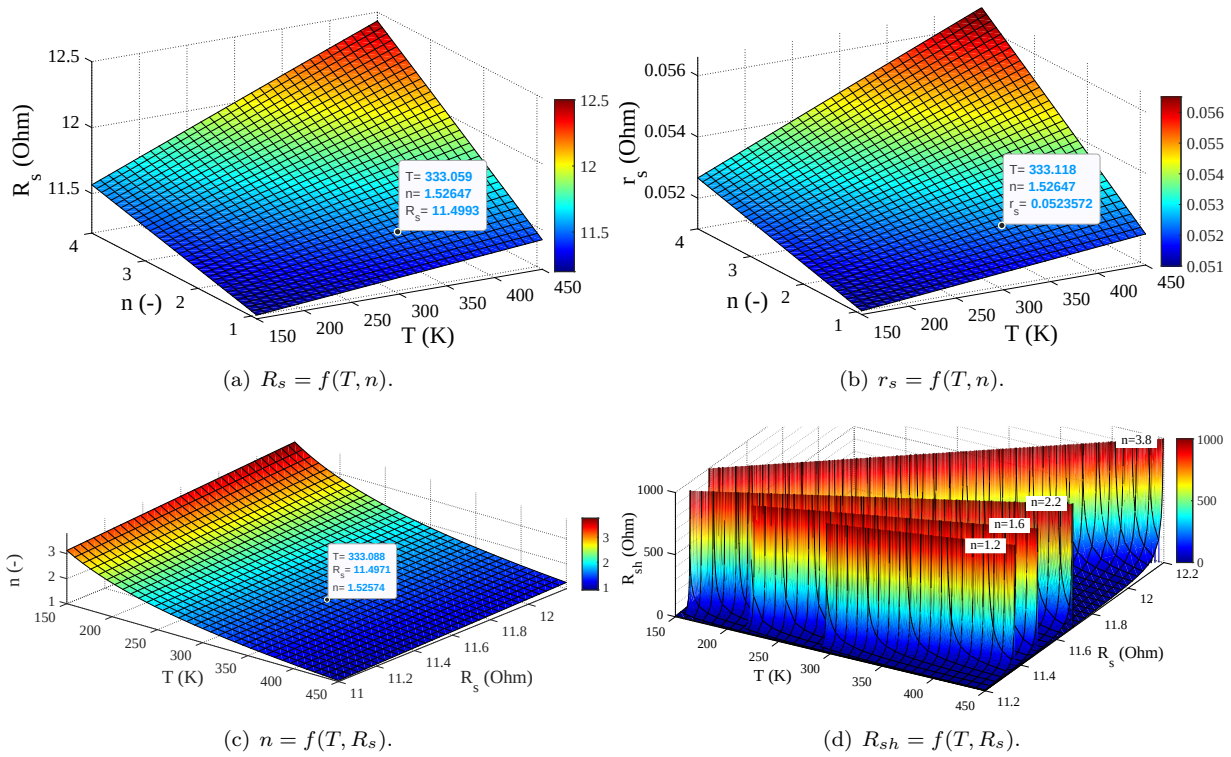
where $q = 1.602 \cdot 10^{-19}$ C is electrical charge of the electron, $k_B = 1.3806503 \cdot 10^{-23}$ J·K^{-1} is the Boltzmann constant, W is the Lambert function, $A = \frac{n k_B T}{q}$, $B = V_{MPP} + R_s I_{MPP}$.

Applying externally measured electrical parameters V_{OC}, I_{SC}, V_{MPP}, I_{MPP} of the specified silicon wafer cell in a sparse matrix leads to the required internal resistances results depicted in Fig. 2. In the iterative simulation process, initial pre-estimated ideality factor n was stated from photovoltaics polycrystalline silicon wafer cells values. Depending on external operational conditions, it typically achieves ranges $n \in (0.9 \ldots 1.3)$ in monocrystalline, $n \in (1.2 \ldots 1.7)$ in polycrystalline and $n \in (1.2 \ldots 2.5)$ in amorphous wafers, at standard operational conditions.

The simulated series resistance R_s results into the range of $R_s = (11.2...12.4)\ \Omega$. To achieve comparability with other dimensionality polycrystalline cells of the same structure, the area size S and R_s values are normalized to r_s per 1 cm^2 per characteristic resistance in this work, via Eq. (9). Both simulations, the R_s in Fig. 2(a) and the normalized r_s in Fig. 2(b), achieve nearly linear profiles within the temperature interval. Very slight resistances rising at the higher temperatures and ideality factor values are mainly caused by the direct thermal heating, i.e., the higher electron mobility, thus band gap contraction for the wafer cell.

Since the ideality factor n is a crucial life-cycle electrical parameter of a wafer cell, it is practical to estimate its behaviour for the same wafer structure. The simulated ideality factor n behaviour depicted in Fig. 2(c) corresponds with above-mentioned ranges and parameters, as can be seen from the inserted labels.

In Fig. 2(d), the very steep behaviour of the shunt resistance R_{sh} is depicted. Based on the previously estimated $n = 1.526$ at the operating temperature $T = 333.15$ K, obtained from the experimental measurements and calculations, the wafer cell should operate in a limited temperature range, following the only fan leaf. However, as from Fig. 2(c), the ideality factor is not a constant. Consequently, the behaviour dynamically "shifts" to either higher or lower n leafs, like indicated in the fan graph in Fig. 2(d), where the only four leaves are illustrated from the whole “constellation of n behaviour”, for the ideality factors $n = \{1.2, 1.6, 2.2, 3.8\}$. Furthermore, R_{sh} is very strongly associated with the behaviour of R_s, both dependent on temperature as well as structural or degradation defects. Assuming a small shift of n value, any small change of R_s is accompanied by an extreme decrease of R_{sh} from $\times$ kΩ values to $\times 10\ \Omega$. This rapid decrease of R_{sh} comes up to curvature that represents the saturation area of the p-n junction, up to the region of the electronic breakthrough. At very low R_{sh}, a high current can cause permanent damage of an electrical component. In Fig. 2(d), again, the size S of the cell wafer plays crucial role in the R_{sh} values. The numerical calculations run up to 16 kΩ border disconti-



(a) $R_s = f(T, n)$. (b) $r_s = f(T, n)$.

(c) $n = f(T, R_s)$. (d) $R_{sh} = f(T, R_s)$.

Fig. 2: Behaviour of the polycrystalline silicon wafer cell intrinsic resistances.

nuity, followed by some dark-claret singularities under the maximal values. The singularities and subsequent area are pre-excluded. It is supposed that the R_{sh} electronic control might lead to a high level of controlled green energy production in smart technologies.

2.3. Complex Impedance and Frequency Response Behaviour

Any silicon wafer structure abounds in inter-layers transition C_T and diffusion C_D capacitances. Such parallel circuit is investigated via theory of electrical systems, by transfer function. Its complex impedance $\dot{Z}_{syst}$ composed of real and capacitive imaginary parts is given by Eq. (10):

$$\dot{Z}_{syst} = \\ = \left[R_s + \frac{R_p}{(\omega R_p C_p)^2 + 1}\right] - j\left[\frac{\omega R_p^2 C_p}{(\omega R_p C_p)^2 + 1}\right] \quad (\dot{\Omega}), \tag{10}$$

where R_p is parallel resistance in (Ω), C_p is parallel capacity in (F), ω is angular frequency in (rad·s^{-1}).

Behaviour of the specified polycrystalline silicon wafer cell is depicted in Fig. 3(a) by Bode diagram, with respect to its frequency responses. The Bode diagram magnitude-frequency line rises from -40 dB with a $+20$ dB·dec^{-1} slope up to cut-off frequency $\omega_{cut} = 1.3$ rad·s^{-1}. Then, it settles to 0 dB i.e. lossless transmission, typical for ideal parallel RC resonant circuits or wideband pass filter. The system does not significantly affect the phase within the investigated frequency band.

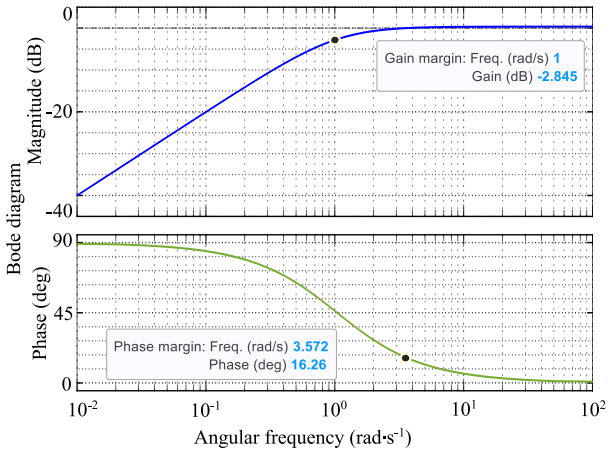
The real versus capacitive imaginary parts behaviour indicates coincidence between simulated results and impedance spectroscopy measurements. The operational range of $R_{sh} \in (10...1000)$ Ω is stated from previous simulations and measurements. As from previously calculated Bode diagram of the specified wafer cell, the angular frequency band spreads from zero at maximum real part of impedance $Re_{\max}$ to the maximum angular frequency of about $\omega = 22.4$ rad·s^{-1} at minimum real part of impedance $Re_{\min}$.

The frequency responses of real and imaginary impedance parts both in Fig. 3(b) and Fig. 3(c) are obtained from the silicon wafer resonant frequency ω_{res} correlation with external reference voltage V_{ref} oscillating at frequency ω_{ref}, based on Eq. (11) and Eq. (12):

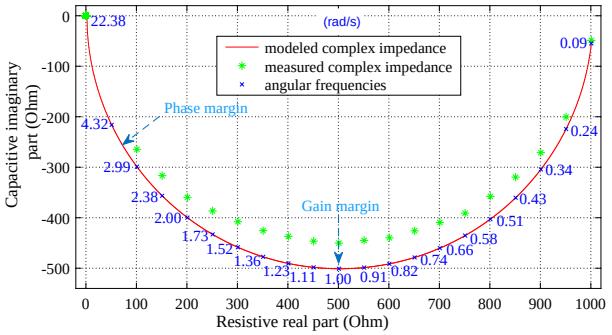
$$Re(V_{ac\,resp}) = \frac{1}{T}\int_0^T \frac{V_{ref\,\max}}{\sqrt{2}} \sin(\omega t + \varphi_{in}) \sin(\omega t) = \\ = \frac{V_{ref\,\max}}{2\sqrt{2}} \cos(\varphi_{in}) \quad (\Omega), \tag{11}$$

$$Im(V_{ac\,resp}) = \frac{1}{T}\int_0^T \frac{V_{ref\,\max}}{\sqrt{2}}\sin(\omega t+\varphi_{in})\cos(\omega t) = \\ = \frac{V_{ref\,\max}}{2\sqrt{2}}\sin(\varphi_{in}) \quad (\Omega). \tag{12}$$

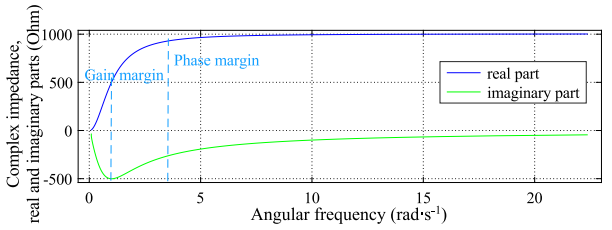
As can be seen from the results, the single-frequency silicon wafer structure reaches the resonant peak and slowly decreases along with the frequency. Such behaviour is typical for narrow-band crystal resonant filter. However, Fig. 3(b) indicates the deviation of the ideally simulated capacitive part from the measured values up to 10 %, caused by drift currents leakage and structural inhomogeneity of the wafer cell.



(a) Bode diagram.



(b) Real and imaginary parts relations.



(c) Impedance parts dependence on angular frequency.

Fig. 3: Complex parameters of the polycrystalline silicon wafer cell.

3. Conclusion

In this work, electrical resistive parameters analysis methodology was stated and generalized, using the specified polycrystalline silicon wafer cell. Five common approaches of the silicon band gap behaviour were compared. The external electrical parameters set $\{V_{OC}, V_{MPP}, I_{SC}, I_{MPP}\}$ of a specified polycrystalline silicon wafer cell was measured at preferred operational temperature interval and used to estimate $\{n, R_s, r_s, R_{sh}, Re, Im\}$ intrinsic parameters relations and their behaviour at wide common temperature interval $T = 150...450$ K or up to extremals. Finally, frequency responses were estimated within operational range. Such iterative modelling and simulation indicate effective way to estimate highly appreciated intrinsic electrical parameters behaviours and their stability control in photovoltaics, optoelectronics, microelectronics or telecommunications.

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Author Contributions

C.G. developed the ideas formulation and research conceptualization, supervised the project, developed the methodology, developed the software models and performed its simulations to visualize achieved results, verified the simulated results by experimental measurements from real silicon wafer, analysed outputs, managed the writing and administration procedures of this work.

References

[1] RUNYAN, W. R. and T. J. SHAFFNER. *Semiconductor measurement and instrumentation*. 2nd ed. New York: McGraw-Hill, 1998. ISBN 978-0-070-57697-1.

[2] WOLF, M. and H. RAUSCHENBACH. Series resistance effects on solar cell measurements. *Advanced Energy Conversion*. 1963, vol. 3, iss. 2, pp. 455–479. ISSN 0365-1789. DOI: 10.1016/0365-1789(63)90063-8.

[3] SHIMURA, F. Single-Crystal Silicon: Growth and Properties. In: *Springer Handbook of Electronic and Photonic Materials*. 2nd ed. Cham: Springer, 2017. ISBN 978-3-319-48931-5. DOI: 10.1007/978-3-319-48933-9_13.

[4] KAKIMOTO, K., B. GAO, S. NAKANO, H. HARADA and Y. MIYAMURA. Silicon bulk growth for solar cells: Science and technology. *Japanese Journal of Applied Physics*. 2017, vol. 56, iss. 2, pp. 1–9. ISSN 1347-4065. DOI: 10.7567/jjap.56.020101.

[5] HUMADA, A. M., M. HOJABRI, S. MEKHILEF and H. M. HAMADA. Solar cell parameters extraction based on single and double-diode models: A review. *Renewable and Sustainable Energy Reviews*. 2016, vol. 56, iss. 1, pp. 494–509. ISSN 1364-0321. DOI: 10.1016/j.rser.2015.11.051.

[6] AUSLENDER, M. and S. HAVA. Single-Crystal Silicon: Electrical and Optical Properties. In: *Springer Handbook of Electronic and Photonic Materials*. 2nd ed. Cham: Springer, 2017. ISBN 978-3-319-48931-5. DOI: 10.1007/978-3-319-48933-9_21.

[7] IRVIN, J. C. Resistivity of Bulk Silicon and of Diffused Layers in Silicon. *Bell System Technical Journal*. 1962, vol. 41, iss. 2, pp. 387–410. ISSN 0005-8580. DOI: 10.1002/j.1538-7305.1962.tb02415.x.

[8] SUNDARAMAHALINGAM, S., A. GURUSAMY, N. SOMI GANESAN, K. VENKATACHALAM and R. PERUMALSAMY. Simulation and Experimental Approach to Investigate the Annealing Effect on mc-Si Ingot Grown by Directional Solidification Process for PV Application. *Silicon*. 2020, pp. 1–12. ISSN 1876-990X. DOI: 10.1007/s12633-020-00604-0.

[9] UMAKANTH, V., S. AJIT, K. SANJAI, T. NEERAJ, V. K. KAUL and P. K. SINGH. A Simulation Study for Optimizing Grain Size in Poly-Crystalline Silicon Material Using Impedance Spectroscopy. *Silicon*. 2021, pp. 1–13. ISSN 1876-990X. DOI: 10.1007/s12633-020-00837-z.

[10] ZAIDI, B., B. HADJOUDJA, B. CHOUIAL, K. KAMLI, A. CHIBANI and C. SHEKHAR. Impact of Hydrogen Passivation on Electrical Properties of Polysilicon Thin Films. *Silicon*. 2018, vol. 10, iss. 5, pp. 2161–2163. ISSN 1876-990X. DOI: 10.1007/s12633-017-9746-3.

[11] SPROUL, A. B. and M. A. GREEN. Improved value for the silicon intrinsic carrier concentration from 275 to 375 K. *Journal of Applied Physics*. 1991, vol. 70, iss. 2, pp. 846–854. ISSN 0021-8979. DOI: 10.1063/1.349645.

[12] MISIAKOS, K. and D. TSAMAKIS. Accurate measurements of the silicon intrinsic carrier density from 78 to 340 K. *Journal of Applied Physics*. 1993, vol. 74, iss. 5, pp. 3293–3297. ISSN 0021-8979. DOI: 10.1063/1.354551.

[13] ALTERMATT, P. P., A. SCHENK, F. GEELHAAR and G. HEISER. Reassessment of the intrinsic carrier density in crystalline silicon in view of band-gap narrowing. *Journal of Applied Physics*. 2003, vol. 93, iss. 3, pp. 1598–1604. ISSN 0021-8979. DOI: 10.1063/1.1529297.

[14] HARMATHA, L. BALLO, P. BREZA, J. PISECNY, P. and M. TAPAJNA. Properties of Si-SiO2 interfaces in MOS structures within nitrogen-doped silicon. *Advances in Electrical and Electronic Engineering*. 2006, vol. 5, iss. 1, pp. 334–336. ISSN 1804-3119.

[15] NAAMA, S., T. HADJERSI, A. LARABI and G. NEZZAL. Effect of Silicon Wafer Resistivity on Morphology and Wettability of Silicon Nanowires Arrays. *Silicon*. 2021, vol. 13, iss. 3, pp. 893–899. ISSN 1876-990X. DOI: 10.1007/s12633-020-00511-4.

[16] LATKOVA, M., M. BAHERNIK, M. HOGER and P. BRACINIK. FSM Model of a Simple Photovoltaic System. *Advances in Electrical and Electronic Engineering*. 2015, vol. 13, iss. 3, pp. 230–235. ISSN 1804-3119. DOI: 10.15598/aeee.v13i3.1411.

[17] ZIDI, L., A. MEKEMECHE a M. BEGHDAD. Performance Analysis on Conversion Efficiency of PERC Solar Cell by PC2D Simulation. *Silicon*. 2019, vol. 11, iss. 5, pp. 2479–2485. ISSN 1876-990X. DOI: 10.1007/s12633-019-00127-3.

[18] DAVIDSON, A. J. C., I. GLESK and A. BUIS. Has Silicon Reached It's Limit? *Advances in Electrical and Electronic Engineering*. 2015, vol. 12, iss. 6, pp. 590–598. ISSN 1804-3119. DOI: 10.15598/aeee.v12i6.1227.

[19] SKARVADA, P., P. TOMANEK, P. KOKTAVY, R. MACKU, J. SICNER, M. VONDRA, D. DALLAEVA, S. SMITH and L. GRMELA. A variety of microstructural defects in crystalline silicon solar cells. *Applied Surface Science*. 2014, vol. 312, iss. 1, pp. 50–56. ISSN 0169-4332. DOI: 10.1016/j.apsusc.2014.05.064.

[20] PERNY, M., V. SALY, F. JANICEK, M. MIKOLASEK, M. VARY and J. HURAN. Electric measurements of PV heterojunction structures a-SiC/c-Si. *Journal of Electrical Engineering*. 2018,

vol. 69, iss. 1, pp. 52–57. ISSN 1339-309X. DOI: 10.1515/jee-2018-0007.

[21] PAPEZ, N., A. GAJDOS, R. DALLAEV, D. SOBOLA, P. SEDLAK, R. MOTUZ, A. NEBOJSA and L. GRMELA. Performance analysis of GaAs based solar cells under gamma irradiation. *Applied Surface Science*. 2020, vol. 510, iss. 1, pp. 1–8. ISSN 0169-4332. DOI: 10.1016/j.apsusc.2020.145329.

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