Hybrid Dynamic CML with Modified Current Source (H-MDyCML): A Low-Power Dynamic MCML Style

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Abstract. *With the growing demands of portable devices, it is necessary to pay attention to low-power digital integrated designs. This paper proposes a low-power MOS Current Mode Logic (MCML) design, termed as Hybrid Dynamic Current Mode Logic with modified current source (H-MDyCML). In H-MDyCML circuits, the functions are realized using complementary pass transistor logic which helps to overcome the problem of stacking of transistors in multiple levels. The dynamic current source has also been modified from an NMOS transistor to a PMOS transistor-driven current source which leads to the elimination of the use of CMOS inverter. H-MDyCML circuits are compared with other existing designing styles: Dynamic CML (DyCML), Hybrid DyCML (H-DyCML), and DyCML with modified current source (Dy-CML-NP). The proposed design (H-MDyCML) shows an overall improvement (in terms of Power Delay Product (PDP)) up to 94.77 % compared to DyCML, 52.17 % compared to Dy-CML-NP, and 91.40 % compared to H-DyCML, for single stage circuits.*

Keywords

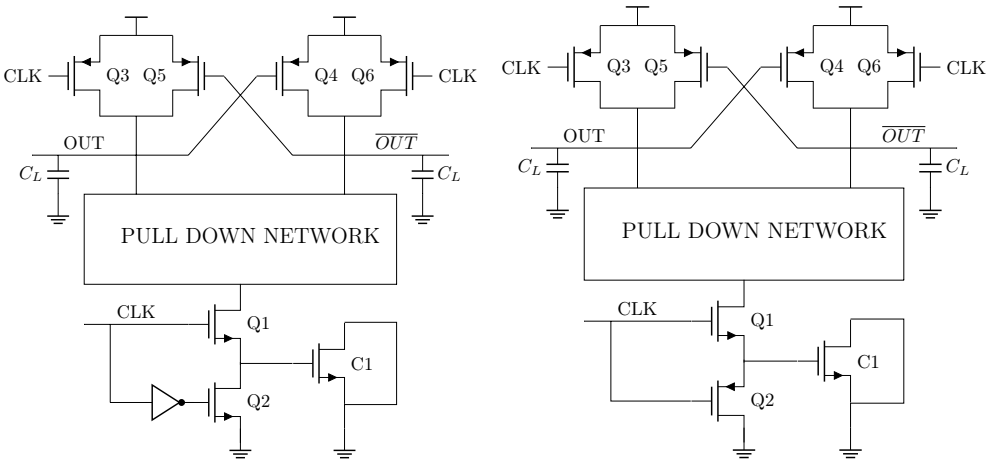
Complementary pass transistor logic, current mode logic, current source, low-power.

1. Introduction

The growth of digital integrated circuits has escalated rapidly in the recent past because of easily accessible Electronic Design Automation (EDA) tools and evolution in technology. This led to a drastic increase in demand for portable electronic goods. One of the major limitations faced by engineers while designing and developing such devices is battery life. Therefore, power dissipation has emerged as an important issue that results in the degradation of the performance of the overall system. To reduce power consumption, researchers are getting inclined towards low-power designs [1], [2], [3], [4] and [5].

Conventional CMOS logic is quite prominently used in digital design due to certain advantages such as high packaging density, negligible static power consumption, and well tested and documented design methodologies. However, while switching, digital circuits based on CMOS logic poses high dynamic power consumption. Switching power dominates the power dissipation in most digital systems which tends to increase at higher operating frequencies drastically. Therefore, there was a shift from CMOS-based digital designs to MCML-based digital designs [6], [7] and [8]. MCML designs have been proved to be a good replacement of CMOS-based designs due to reduced power consumption at high frequencies. However, because of the presence of a static current source, the circuits had static power dissipation accompanied by increased design complexity.

Therefore, there was a further shift from MCML-based circuits to DyCML-based circuits [9] and [10]. This is a newly proposed logic family in the literature that uses a dynamic current source in place of a static current source and works on the pre-charge and evaluation method [11] and [12]. Thus, DyCML circuits help to achieve high performance at lower power dissipation.



(a) Dynamic Current Mode Logic (DyCML). (b) DyCML with modified current mode logic (Dy-CML-NP).

Fig. 1: Basic Architecture of (a) DyCML style [10] and (b) DyCML style with modified current source (Dy-CML-NP) [15].

Nonetheless, the realization of functions with multiple inputs requires stacking of transistors which leads to a significant rise in delay. To overcome this problem, a new method, known as H-DyCML, was proposed recently [13] to avoid stacking of the transistors and hence reduce the delay. This method is based on Complementary Pass transistor Logic (CPL) to implement logic functions. However, there is still significantly high power consumption due to the use of an additional CMOS inverter which is required to obtain an inverted Clock (CLK) signal to drive the NMOS transistor of dynamic current source. Therefore, a method to eliminate the use of a CMOS inverter, namely Dy-CML-NP, has been recently proposed [14] and [15] where NMOS transistor in dynamic current source of a DyCML circuits has been replaced by a PMOS transistor which is driven by CLK signal instead of an inverted CLK signal. However, Dy-CML-NP also poses a limitation due to stacking of transistors. Therefore, this paper proposes a new method that overcomes the limitation of H-DyCML and Dy-CML-NP, and exploits the advantages of both methods by combining them.

The remaining article has been organized as follows: Sec. 2. traces the background of research emphasizing on importance, working, advantages and disadvantages of circuits designed using DyCML, H-DyCML, and Dy-CML-NP. Further, Sec. 3. introduces the proposed low-power design. Cascading of proposed H-MDyCML has been explained in Sec. 4. and Sec. 5. presents the simulation results and comparison of the performance of various other designing styles with proposed style. Then finally, the paper is concluded in Sec. 6.

2. Background

In MCML-based circuits, the use of a constant current source and reduced voltage swing results in lower dynamic power consumption but also brings with it certain drawbacks which limit its usage. Static power dissipation is the major drawback faced by engineers in designing systems using MCML logic. Therefore, to overcome this issue, there was a shift from MCML-based logic to DyCML-based logic [10] wherein a dynamic current source was used. A typical architecture of a DyCML circuit is shown in Fig. 1(a). DyCML circuits follow the principle of pre-charge and evaluation which exists in dynamic logic circuits.

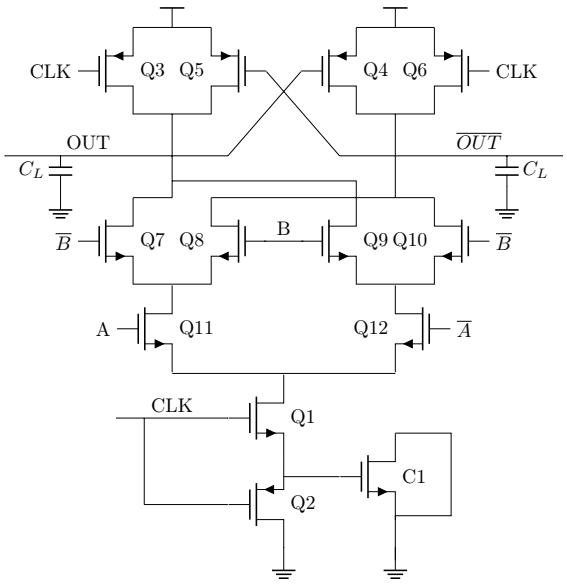


Fig. 2: Realization of XOR gate using DyCML with modified current source (Dy-CML-NP) [15].

One of the major changes made from MCML circuits was that the pull-up network was changed to active loads (Q3 and Q6) connected along with cross-coupled latches (Q4 and Q5) instead of load resistors only. Another major change made from MCML circuits was the replacement of static current source to dynamic current source built using NMOS (Q2) driven by inverted CLK signal. However, the logic function was evaluated similarly to that in MCML: using the 'Pull Down Network' block.

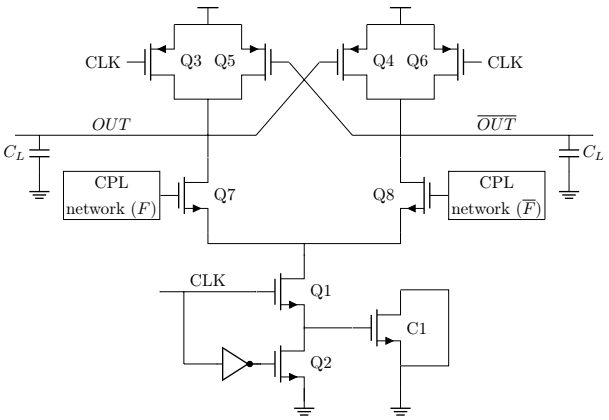


Fig. 3: Basic architecture of H-DyCML style [13].

Due to the presence of a dynamic current source in DyCML circuits, power was saved significantly along with increased performance as compared to MCML-based logic gates. However, the use of a CMOS inverter to obtain an inverted CLK signal that drives the NMOS transistor in the dynamic current source still contributed to high dynamic power dissipation. Therefore, to address this issue, a new method (Dy-CML-NP) was recently introduced in [15] which suggests to modify the dynamic current source in DyCML circuits by replacing the NMOS transistor with a PMOS transistor. Basic architecture of Dy-CML-NP is shown in Fig. 1(b), and it is evident that the requirement of the inverted CLK signal has been withdrawn. Although the issue of power dissipation has been addressed in Dy-CML-NP designing style, yet the delay remains critical due to multiple levels of stacking of transistors in the pull-down network which additionally increases the delay of a gate. This could be better understood by the design of 2-input XOR gate shown in Fig. 2. There are two levels of source-coupled transistors such that each input and its complement is applied to their gates. Therefore, the problem of stacking persists for both DyCML and Dy-CML-NP circuits. To overcome the problem of stacking of transistors in multiple levels, a new method was recently proposed in [13]. This method of designing, termed as H-DyCML, made use of complementary pass transistor logic to solve the issue. The working of H-DyCML-based logic can be explained with the help of Fig. 3. It also follows the pre-charge and evaluation method in a similar manner as in DyCML-based logic. The difference lies in the way a function was realized. The pull-down network in H-DyCML circuits consists of one level source-coupled NMOS transistor only such that their gate terminals are driven by the output of a CPL logic which is built using NMOS transistors.

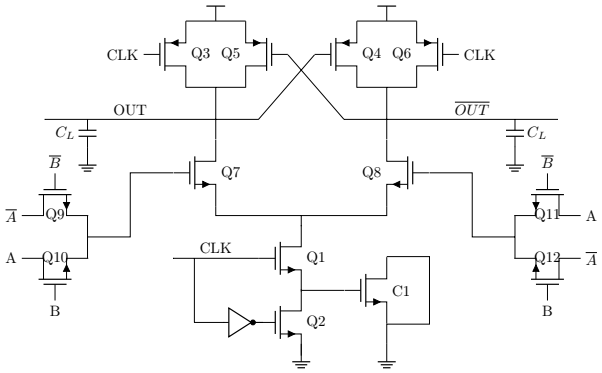


Fig. 4: Realization of XOR gate using H-DyCML style [13].

This is better enlightened in Fig. 4 which realizes 2-input XOR gate using H-DyCML style. Transistors Q9 and Q10 implement the function $\overline{A \oplus B}$ and Q11 and Q12 implement the function $A \oplus B$. If the output of the implemented logic $A \oplus B$ is HIGH, then Q7 is turned OFF and Q8 is turned ON. From this reason, OUT terminal is directly connected to the ground and OUT stays at V_{DD}. Since, NMOS transistors offer weak pull-up and strong pull-down, the maximum voltage level at the output of NMOS pass transistor (V_{OH}) is equal to gate voltage (V_{DD}) reduced by one threshold voltage (V_{tn}), that is, $V_{OH} = V_{DD} - V_{tn}$. Therefore, to avoid erroneous results, three techniques have been proposed in [13]:

- Use of level restorer circuit.
- Use of Multiple threshold voltage transistors.
- Use of transmission gates.

3. Proposed H-DyCML Circuits with Modified Current Source (H-MDyCML)

In this section, the proposed structure (H-MDyCML) for low-power, high-speed designing has been elaborated which jointly exploits the advantages of both H-DyCML and Dy-CML-NP designing styles. The proposed designing style has shown improvement in terms of:

- Delay when compared to Dy-CML-NP and DyCML.
- Power when compared to DyCML and H-DyCML.
- PDP when compared to DyCML, Dy-CML-NP, and H-DyCML.

Above improvements are supported by proper results and explanations in rest of the paper. Basic architecture of H-MDyCML circuits is shown in Fig. 5 and its working can be understood as explained further. The operation of the circuit still follows the pre-charge and evaluation mechanism as earlier. In the pre-charge phase, when CLK = LOW, transistors Q3, Q6, and Q2 are switched ON. Therefore, the load capacitors are charged to V_{OH}=V_{DD} through active loads (Q3 and Q6), and capacitor C1 is discharged through Q2. However, one thing to be noted here is that PMOS has a weak pull-down property which is why the capacitor discharges up to a level $V = V_{tp}$ because beyond that PMOS is switched OFF. Thus, capacitor C1 does not discharge to ground potential, but to one threshold voltage level above the ground potential. During the pre-charge phase, the output levels remain at V_{OH} and are unaffected by the inputs applied to the CPL logic because Q1 is switched OFF which disconnects the output nodes from capacitor C1. At this time, cross-coupled latches (Q4 and Q5) are also disconnected.

In the evaluation phase, when CLK = HIGH, transistors Q3, Q6, and Q2 are switched OFF. Q1 is switched ON and offers a direct path between output nodes and capacitor C1 which acts as a virtual short. However, C1 already contains some charge on it due to the weak pull-down nature of PMOS, as is explained above. During the evaluation phase, the values of inputs applied to CPL logic are evaluated. Since the two CPL functions implemented are the complement of each other, therefore, when the output of one CPL logic is HIGH, the output of another CPL logic is LOW which leads to discharging of one output node to $V_{DD} - V_{swing}$ and other remaining at V_{DD}. The output nodes are maintained at these levels with the help of latches built using cross-coupled PMOS transistors (Q4 and Q5). At the same time, the voltage across the capacitor goes from V_{tp} to $V_{DD} - V_{swing}$. The value of capacitor C1 is decided by the equation, as given in [15]:

$$C1 = \frac{V_{swing}}{V_{DD} - V_{swing} - |V_{tp}|} \cdot C_L. \qquad (1)$$

The reason for the subtraction of $|V_{tp}|$ in the denominator has been explained above; capacitor C1 is already charged to a potential of $|V_{tp}|$ after the pre-charged phase. For better understanding, 2-input XOR gate has been realized using H-MDyCML style as shown in Fig. 6.

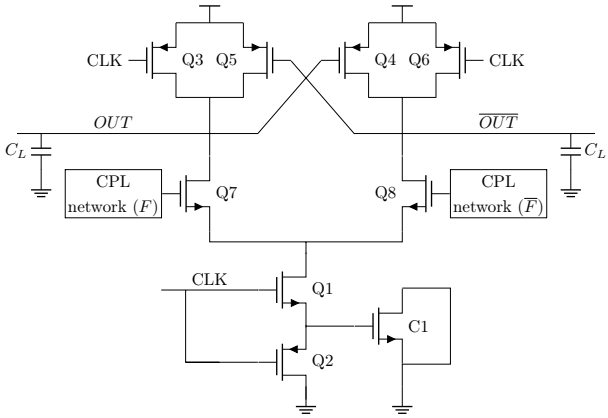


Fig. 5: Basic architecture of H-MDyCML style.

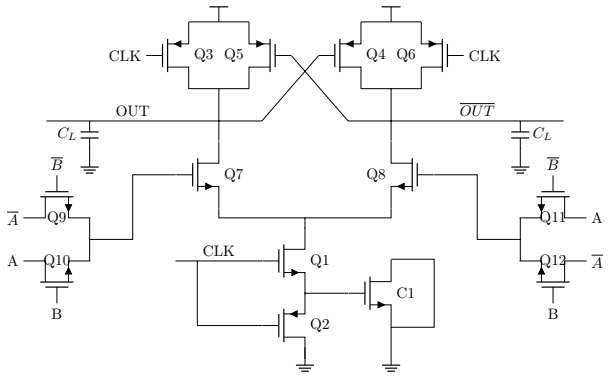


Fig. 6: Realization of XOR gate using H-MDyCML style.

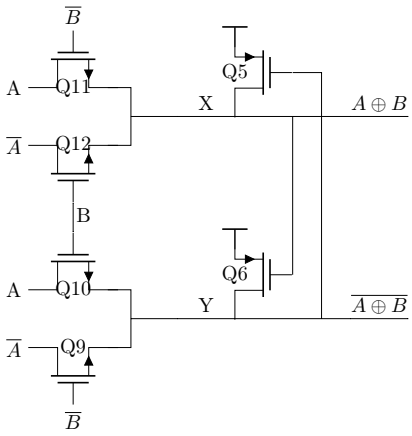


Fig. 7: Technique of level restoring [11] and [13].

Out of 3 techniques proposed in [13] to maintain the output of CPL logic at V_{DD} to avoid erroneous results, we choose the first technique of level restorer. It employs two cross-coupled PMOS transistors as shown in Fig. 7 which act as weak pull-up transistors. It implements XOR/XNOR functions. If applied inputs are such that the XOR function is set HIGH and XNOR is LOW, then Q5 will be turned ON, pulling up node

X and Q6 will be turned OFF, maintaining node Y at low potential. The reason for choosing this technique is the ease of choosing the voltage swing, that is, we can adjust the swing such that it is greater than the threshold voltage. However, dealing with other techniques increases the complexity and number of transistors utilized. Therefore, the technique of level restorer allows usage of a lesser number of transistors as compared to transmission gate logic without putting any constraint on threshold voltages of CPL logic transistors or level restorer transistors. Thus, the H-MDyCML style presents a good solution for low-power designs as it not only deals with the problem of increased delay due to stacking of transistors, but also helps remove CMOS inverter which is responsible for high dynamic power consumption.

4. Cascading of H-MDyCML Circuits

Simulation of individual gates is relatively simpler and the problem arises when two or more gates need to be cascaded together. The problem that arises while cascading is that the evaluation phase of consecutive stages occurs simultaneously. This results in erroneous results because the second stage starts evaluation before the first stage has finished evaluating inputs. Therefore, a certain delay must be incorporated after the first stage and before the second stage to separate the evaluation phase of two consecutive stages. To accomplish this task, additional circuitry, which act as a bridge, is added between the two stages. The circuitry has been proposed in [15] and looks as shown in Fig. 8 where EOE is the voltage drop across capacitor C1 and CLK is the clock signal of the previous stage. It is the Self-Timed Buffer (STB) similar to that proposed in [10], with a slight modification. Working of the shown STB is explained further.

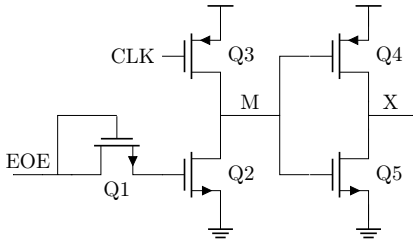


Fig. 8: Self-Timed Buffer [15].

In H-MDyCML circuits, in pre-charge phase, capacitor C1 is discharged to V_{tp} (when CLK = LOW). If we directly apply this signal to Q2, it will switch ON the transistor because $V_{tp} > V_{tn}$. Therefore, an additional NMOS is needed (Q1) which leads to one threshold voltage drop and thus switching OFF Q2. At the same time, Q3 is switched ON charging the node M to V_{DD}. This furthers activates Q5 and deactivates Q4 such that node X is subsequently pulled down to the ground. Similarly, in the evaluation phase, the total charge carried by load capacitors (C_L) and capacitor C1 is redistributed such that C1 is charged up to voltage equal to $V_{DD} - V_{swing}$ from V_{tp} (when CLK = HIGH). At this time, transistor Q3 is turned OFF while Q1 and consequently Q2 is turned ON. This pulls down the potential of point M to ground and subsequently, Q4 is turned ON while switching OFF Q5. Node X is charged up to V_{DD}. Therefore, CLK signal is transmitted to point X with some delay. One thing to be noted here is that this STB also eliminates the use of CMOS inverter to obtain the complement of CLK signal. This results in further reduction in dynamic power dissipation. An example of cascading is shown in Fig. 9. It shows a full adder in which two STBs are used. The first STB is used to cascade the first stage XOR gate to the second stage XOR and AND gates. The second STB is used to cascade the output of first and second stage AND gates to OR gate.

5. Simulation Results

Various gates designed using H-MDyCML style are simulated using Cadence Virtuoso. All the circuits are designed using 180 nm CMOS technology parameters. In order to avoid erroneous results at the output of CPL logic, the voltage swing needs to be kept greater than the threshold voltage. Therefore, V_{swing} is chosen to be 700 mV. The supply voltage is chosen as 1.8 V and since V_{swing} is 700 mV, $V_{DD} - V_{swing}$ becomes 1.1 V. Apart from this, C_L is taken to be 40 fF. Using Eq. (1), C1 comes out to be approximately 47 fF. For a fair comparison, various gates are also implemented using designing styles: DyCML, H-DyCML, and Dy-CML-NP in parallel with H-MDyCML. Various circuits used for comparison are: AND, OR, and XOR gates. For all the circuits, the parameters mentioned above are kept the same. However, the value of C1 differs in the case of DyCML and H-DyCML circuits since they use a current source driven by NMOS. The value of capacitor C1 for designing styles with NMOS driven current is source is given by [10]:

$$C1 = \frac{V_{swing}}{V_{DD} - V_{swing}} \cdot C_L. \tag{2}$$

According to Eq. (2) the value of capacitor C1 comes out to be approximately 26 fF for DyCML and H-DyCML. Different parameters compared for all the circuits are: Delay, Power, and PDP whose analysis for AND, OR, and XOR gates is summarized in Tab. 1.

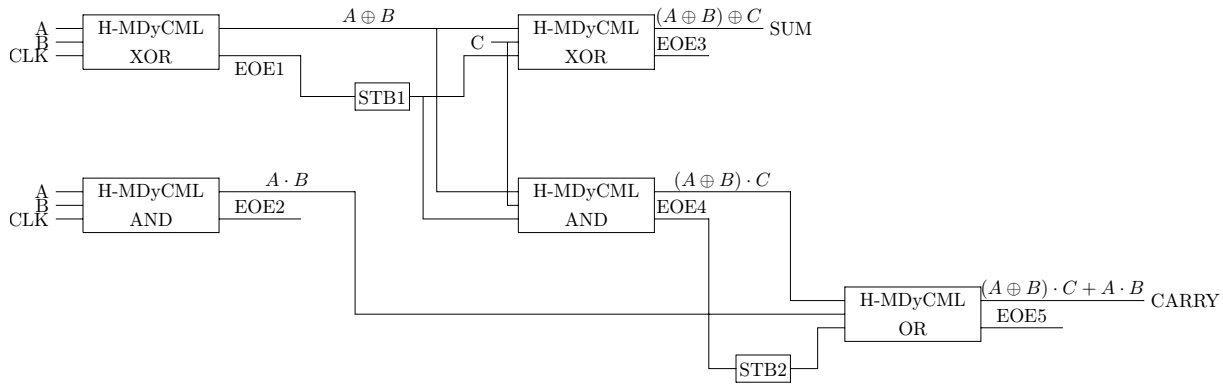


Fig. 9: Cascading required in Full-Adder circuit.

Tab. 1: Performance comparison.

Parameter	Style			
	DyCML	Dy-CML-NP	H-DyCML	H-MDyCML
AND gate				
Power (μW)	2.061	0.117	2.051	0.129
Delay (ps)	287.78	590.80	187.78	254.01
PDP (fJ)	0.593	0.069	0.384	0.033
OR gate				
Power (μW)	2.175	0.119	2.046	0.207
Delay (ps)	276.60	552.87	187.78	248.82
PDP (fJ)	0.602	0.066	0.384	0.052
XOR gate				
Power (μW)	2.073	0.111	2.047	0.129
Delay (ps)	304.92	591.10	182.83	253.09
PDP (fJ)	0.632	0.066	0.374	0.033
Full Adder				
Power (μW)	39.660	36.033	47.701	38.352
Delay (ps)	2646.39	2943.61	2615.65	2150.88
PDP (fJ)	104.956	106.068	124.769	82.492

Following observations can be made from the Tab. 1:

- H-MDyCML gates have less power consumption as compared to DyCML and H-DyCML gates due to the elimination of CMOS inverter. However, power consumption in H-MDyCML is greater than Dy-CML-NP due to the use of additional power supply in level storing circuit of CPL network.
- H-MDyCML gates have reduced delay as compared to DyCML and Dy-CML-NP gates due to replacement of stack of transistors with a CPL network to realize the logic. But, delay of H-MDyCML is greater than that of H-DyCML due to higher value of capacitor C1 in case of H-MDyCML, calculated using Eq. (1).
- PDP is the lowest for the proposed method due to combined effect of power and delay, which means that overall performance of the proposed designing style is better than others.

Apart from simulating individual gates, a full adder is designed, as shown in Fig. 9, and compared to show the effects of cascading on the performance of designs using different designing styles. The results for a full added for the same parameters as in the previous case are also recorded in Tab. 1 where it can be seen that the delay of the proposed H-MDyCML design is less than DyCML and Dy-CML-NP designs, and the power is less than DyCML and H-DyCML designs. Moreover, its PDP is the least. Therefore, it can be concluded that for single stage circuits, H-MDyCML shows an overall improvement (in terms of PDP) up to 94.77 %, 52.17 % and 91.40 % compared to DyCML, Dy-CML-NP and H-DyCML respectively. Also, H-MDyCML style shows an average improvement of 25.83 % from other designing styles in case of Full-Adder circuit. Decreased improvement with increasing stages in circuit is due to power and delay introduced by STBs.

Furthermore, the variation of performance of various designing styles has been observed with increasing voltage swing. Figure 10, Fig. 11 and Fig. 12 summarize the results for variations in delay, power, and PDP respectively with changing voltage swing for different designing styles. To analyze these variations, a 2-input

XOR gate is considered. Few things can be observed from the graphs in Fig. 10, Fig. 11 and Fig. 12:

- Delay shows an upward trend with increasing voltage swing (V_{swing}) for all designs because more charge needs to be transferred from load capacitors (C_L). The increase in delay across the domain of V_{swing} is significantly low, up to an average of 16.16 ps, which is evident from Fig. 10.

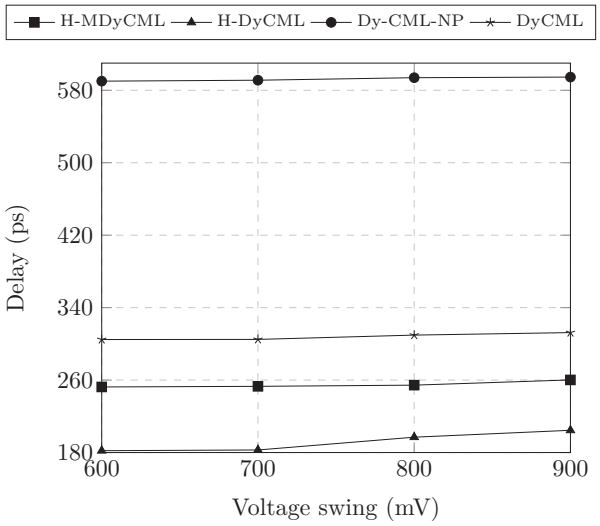


Fig. 10: Delay of a 2-input XOR gate realized using different styles with varying voltage swing (V_{swing}).

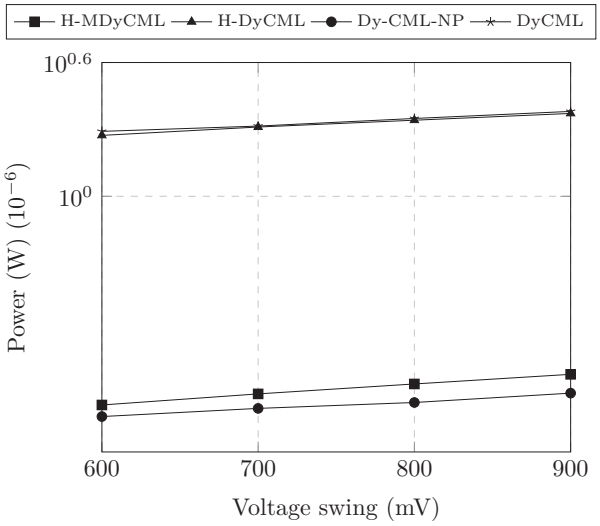


Fig. 11: Power of a 2-input XOR gate realized using different styles with varying voltage swing (V_{swing}).

- Power dissipation increases with increasing voltage swing for all designs because it is directly proportional to the V_{swing}.
- PDP increases with increase in voltage swing in case of all four designing styles due to the increase in power and delay. Moreover, PDP is the least for H-MDyCML style due to combined effect of improved power and delay.
- Difference between power dissipation of H-DyCML (or DyCML) and H-MDyCML increases with increasing voltage swing. This happens because power in H-DyCML and H-MDyCML circuits are of order 10^{-6} and 10^{-7} respectively. Since power is directly proportional to V_{swing}, absolute increase in power for H-DyCML is more than H-MDyCML. Similar trend is observed for PDP as it is directly proportional to power. Thus, improvement becomes more significant as V_{swing} is increased.

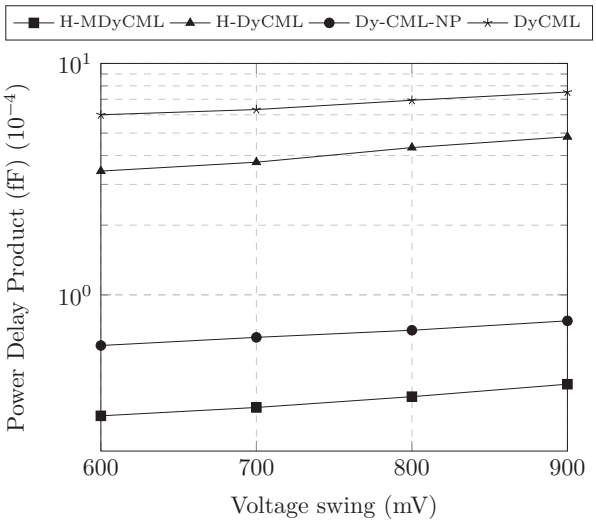


Fig. 12: PDP of a 2-input XOR gate realized using different styles with varying voltage swing (V_{swing}).

6. Conclusion

In this paper, a new method is proposed to design dynamic low-power, high-speed circuits. The new method combines the structure of H-DyCML and Dy-CML-NP to have reduced power consumption and delay. The reduced power consumption is possible due to the elimination of a CMOS inverter by using a dynamic current source built using a PMOS transistor as proposed in Dy-CML-NP circuits. The delay has been reduced due to use of the complementary pass transistor logic instead of a stack of transistors. Different gates are designed using DyCML, H-DyCML, Dy-CML-NP, and H-MDyCML styles and compared with each other in terms of power dissipation, delay, and power delay product. Therefore, it will be right to conclude that the circuits designed using the proposed method have better overall performance as compared to other methods.

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