Switching Losses Analysis of a Constructed Solar DC-DC Static Boost Converter

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Abstract. *The DC-DC converter is majorly used in several renewable energy applications. It is usually relevant in a hard-switching operating mode at the cost of increasing power losses and declining efficiency. Power losses are comprised of switching losses and conduction losses, which affect the reliability and speed up the aging of the switch. Therefore, soft-switching techniques are inescapable to reduce electromagnetic interference EMI, minimize losses, and enhance power conversion efficiency. Among the sundry techniques of soft-switching, passive snubbers are uncomplicated and vigorous, besides it has been spotlighted as a finer alternative compared to the active snubbers that involve extra switches and an additional control circuit. This paper investigates the power loss of a conventional solar DC-DC static converter designed and controlled through Maximum Power Point Tracking (MPPT). It evaluates the switch's temperature in the hard-switching operating mode. Besides, this paper presents a new research initiative that aims to allow a zero switching and stabilizing the temperature of the switch through a novel approach of design for RLD and RCD snubber cells. This new design allows the switch to achieve soft-switching, by abolishing the voltage stress, minimizing the power losses, and stabilizing the junction temperature. This snubber has a simple structure with a few components and ease of control, which helps to upgrade the power conversion efficiency through controlling the high voltage and current stress in the switch. In this treatise, elements of the snubber are designed and adjusted for maximum reliability through the simulation in OrCAD environment. Furthermore, the effectiveness of the model is approved through experimental results on a 1600 W conventional boost to validate the proposal.*

Keywords

Continuous Conduction Mode (CCM), DC-DC converter, Passive snubber, Soft-switching reverse-recovery loss, Zero Current Switching (ZCS), Zero Voltage Switching (ZVS).

1. Introduction

In recent years, renewable energy has presented a high development, assignable to the inexhaustible resources, and the lowest environmental effects. Furthermore, day to day, the development of renewable energy resources is based essentially on the power electronics applications [1] and [2].

The DC-DC boost converter has been highlighted in numerous research so far for distinct purposes which allow good controllability, simple and inexpensive design to implement [3] and [4]. The classical converter, as can be seen in Fig. 1, is usually used in a hard-switching operating mode occurring switching losses. Moreover, higher switching frequency increases switching losses along with the electromagnetic interface. The conventional hard-switching converters are still an adequate choice for improving the power density, efficiency, reliability, and cost for regular commercial applications. However, the converters supplied with renewable energy sources, mainly photovoltaic panel sources, are recognized by their significant low yield. Therefore, this type of application needs the following design specifications: reduction of EMI, minimization of power losses, and stabilization of junction temperature. These lead to increased efficiency of such converters. To address these problems, soft-switching techniques are incited instead of hard-switching [5], [6] and [7].

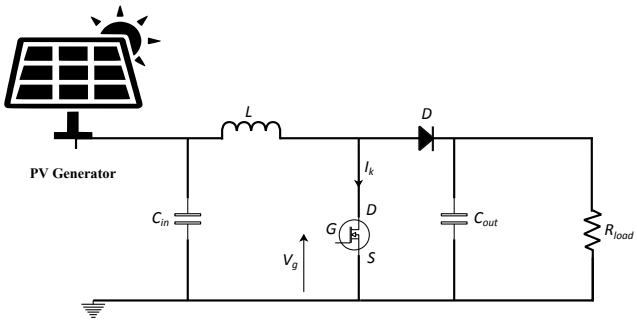


Fig. 1: DC-DC conventional boost converter.

Power losses in the boost converters are resulting from two major sources: conduction loss and dynamic loss. These power losses lead to overheating that impacts the reliability and contributes to accelerated aging of interrupters. To eschew these power losses, several snubbers have been recommended to limit the rate of change in voltage $\frac{dv}{dt}$ or current $\frac{di}{dt}$ and overvoltage during the turn on/off. These various snubbers are classified into active and passive snubber.

As treated in [8] and [9], the active snubbers are employed to minimize the turn-on switching losses. The majority proposed in the literature uses an auxiliary switch that involved an intermediate interface control circuit. The synchronization problems among control signals of the switches during transients increase the complexity of the control strategy, circuit's size, and the cost. Over and above, the proposed active snubber provides soft-switching operation for the main switches and reduces the voltage stress of the main switches. However, the voltage stress of the main diode is twice the output voltage, and the auxiliary devices are operated by hard-switching. Hence, the snubber elements cause extra switching power losses. In [13], Zero Voltage Transition (ZVT) is achieved for high set-up interleaved switches, but there is a transformer in the auxiliary circuit. The leakage inductance causes additional losses in this converter. However, passive snubbers have low cost, easy control and application. There are some downsides needed to be controlled in passive snubber cells. In [5], Zero Voltage Switching (ZVS) is not able to accomplish perfect turned off, despite Zero Current Switching (ZCS) can realize a correct turn on. While in [10], it provides semi-ZCS for the turning on. The switching losses cannot be totally eliminated in both studies. In [11], the increasing number of components in the snubber cell leads to a higher cost and makes the application more complex. Besides, some snubber circuits are particularly made for their own converter structure, and hence, they cannot be applied to the family of fundamental DC-DC converters [12].

In the previous research quoted above [5], [6] and [7], RLD and RCD snubbers are presented as a solution to minimize the losses. As a drawback, they reduce the switching losses partially but they do not eliminate the total of the switching losses. This paper presents a new approach to design the snubber cells that provide perfectly a soft-switching, a zero voltage switching turn on, and a zero current switching turn off together for the main switch of the DC-DC converter by using only resonant circuit RCD and RLD.

The snubber cell has a simple structure; it requires merely passive components and results in higher reliability, smaller size, lower weight, coast, and ease of control. The proposed circuit is implemented to a renewable energy converter, more precisely solar DC-DC converter, where the high efficiency is considered mainly. In the proposed converter, the switch achieves soft-switching, which abolished the voltage stress, minimized the power losses, and stabilized the temperature's junction of the switch. In this study, the hard-switching properties of the MOSFET are detailed in Sec. 2. In addition, the power losses for the static and dynamic state of the converter are presented in Sec. 3. Besides, the design and theoretical analysis of the proposed converter are made in Sec. 4. Finally, the experimental and simulation results of the proposed converter operating under the hard-switching and the soft-switching are compared in Sec. 5.

2. The Hard-Switching Properties

2.1. Switching on Properties

A forward-biased MOSFET can be turned on by applying a positive voltage between the gate and the source. However, to go from forward blocking mode to forward conduction mode, it takes some transition time t_d. It can be subdivided into three small intervals as delay time, rise time t_r, and time on t_{on}, as shown in Fig. 2.

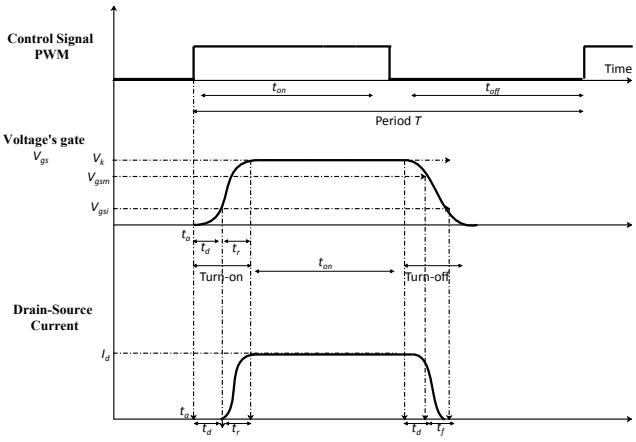


Fig. 2: MOSFET's switching characteristics.

After the application of the gate voltage, the MOSFET will start conducting over a very tiny region t_d. Through delay time, the gate's input capacitance gets charged from 0 V to V_{gsi}, where V_{gsi} is the starting point where the current I_d is in condition to start flowing, but it is not flowing. Rising the gate voltage from V_{gsi} to V_{gsm}, the current I_d starts to drain and achieves the saturation at the value of V_{gsm}, where V_{gsm} is the necessary voltage to drive the MOSFET to turn-on condition. This period is defined as the rise time where the switch tries to reach the turn-on and it is the genesis of the switching turn-on loss E_{on}. Afterward, the switch gets fully turn-on for a period t_{on}.

2.2. Switching off Properties

The switching-off started at the t_b, once the gate voltage is eliminated. It can be divided into two intervals, as shown in Fig. 2, the delay time for the turning-off, t_{df}, and the fall time, t_f. The turn-off is defined as the duration where the switch is getting off and contributes to the switching loss. While the delay turn-off t_{df}, the gate's input capacitance discharges from the over-drive gate voltage V_k to V_{gsm}. However, the current stands constant until V_{gsm}. Afterward, while the fall time t_f, the input capacitance endures discharging from V_{gsm} to V_{gsi}. Identically the drain current begins to reduce from I_d to zero. So, every time that the drain current I_d gets to zero or the gate voltage reaches lesser than the threshold V_{gsi}, and the turn-off operation gets done.

Therefore, the switching losses arise ascribable to the stored charges. Besides, when the voltage's gate is decreased to a value lower than the threshold V_{gsi}, the process of switching-off is realized. While switching on/off, the MOSFET experiences a decrease of one parameter (voltage or current) and the corresponding increase of the other. This transition is not instantaneous, hence during every turn on and off, there is a finite duration (t_{on}, t_{off}) for which both voltage and current are non-zero. And so, there is power loss in the hard-switching device. The higher the switching frequency, the higher is the loss and the more heat is dissipated. To reduce the switching stress, the switching point of the voltage and the current must be reduced.

3. Power Losses in the Conventional Boost Converter Circuit

The losses in the boost converter are separated into conduction and dynamic losses. While the conduction losses occur when the MOSFET is in full conduction, they are practically resulting from the resistance in the elements of the circuit, such as diode, capacitors, inductor, and MOSFET. Yet, the dynamic losses represent a considerable part of losses. They occur in every transition period of the switching. These losses are directly proportional to switching frequency and the less dependent on the load, which means the higher the frequency, the higher the losses.

The equivalent schema of the DC-DC converter is given in Fig. 3. With certain assumptions, presented as follow, the converter elements are independent in time, temperature, frequency, and they are linear [13].

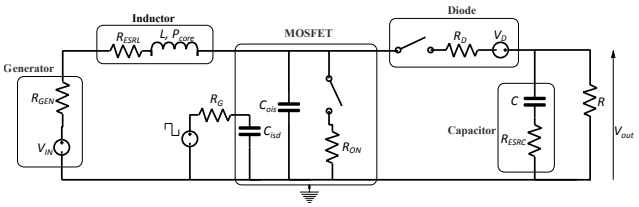


Fig. 3: Equivalent circuit of the DC-DC converter with parasitic elements.

Depending on the switching frequency, duty factor and load, the converter can operate in two different modes, the Continuous Current Mode (CCM) or the Discontinuous Current Mode (DCM). This fact must be taken into account while calculating the current equation for the converter.

3.1. Conduction Losses

To determine the conduction power losses, the average current I_{av} and the effective current I_{eff} are required. These currents are defined as follow:

$$I_{eff} = \sqrt{\frac{1}{T}\int i^2(t)dt}, \tag{1}$$

$$I_{av} = \frac{1}{T}\int i(t)dt, \tag{2}$$

In the continuous current operating mode, the conduction losses in the boost converter are equal to the average power sum in all elements of the circuit, as shown in Fig. 3. It is defined as:

$$\begin{aligned} P_{cond} = R_{gen}I^2_{Leff} + R_{esl}I^2_{Leff} + R_{on}I^2_{TReff} + \\ + R_dI^2_{deff} + V_dI_{dav} + R_{esrc}I^2_{ceff}. \end{aligned} \tag{3}$$

3.2. Dynamic Losses

Dynamic losses occur in the transition period of the switch. The average losses can be calculated as follow:

$$P_{sw} = k\left(t_rI_{lmax} + t_fI_{lmin}\right)V_{out}f_{sw}, \tag{4}$$

where t_r and t_f are the gate voltage rise time and fall time, respectively. V_{out} is the voltage across the switch during the turn-on and the turn-off, and f_{sw} is the switching frequency.

In the boost converter, the semiconductors represent the most lossy elements in the circuit. The turn on/off time of the switch is in the range of a few tens of nanoseconds to multifold microseconds. During these switching transitions, very high power losses can occur in the semiconductor device. Although the switching time of semiconductor elements is very short, average power loss can be substantial. Dynamic losses are very little dependent on power load but directly depend on switching frequency. As Fig. 4 unveils, the dynamic losses in the switch are predominant compared to the conduction losses. For this reason, reducing the switch losses will gain less power loss by the circuit.

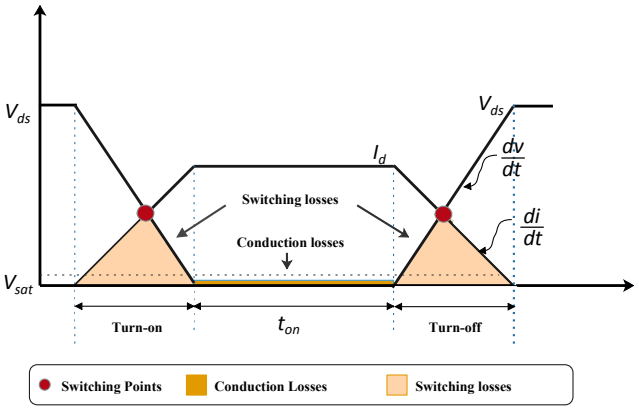


Fig. 4: Device voltage and current during hard-switching transients.

4. The Proposed Snubber Circuit and Its Operation

The MOSFET utilized in power converters operate usually in the hard-switching mode. The dynamic behavior of power semiconductor devices attracts attention, especially for the faster ones, for a number of reasons: optimum drive, power dissipation, EMI/RFI issues, and the junction's temperature [14]. The hard-switching refers to the stressful switching behavior of the power electronic devices during the turn-on and the turn-off processes. The device has to withstand high voltage and current simultaneously, which engenders a high switching loss and stress [6]. One of the biggest challenges connected to hard-switching is certainly connected to the fast-changing of $\frac{dv}{dt}$ and $\frac{di}{dt}$, causing the electromagnetic noise generated in the switching moment, as the frequency rises, the noise frequency gets higher [15].

4.1. Proposed Passive Snubber Circuit

Several varieties of resonant snubbers structures are proposed by D. Tardiff [17] and W. McMurray [18]. They can be classified into unpolarized snubber circuits and polarized ones. The proposed passive snubber circuit is employed to conserve the semiconductor and minimize the stress in the switch during the switching operations. It assures that the electrical rating of the device does not reach out to the limits of the semiconductor [16].

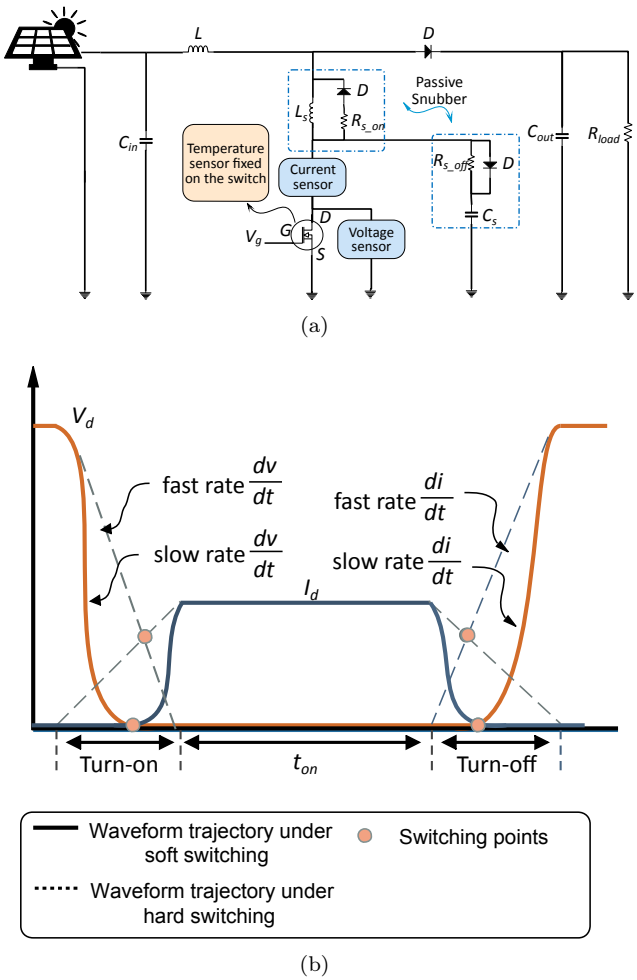


Fig. 5: Solar DC-DC converter with the proposed snubber circuit, (a) soft-switching boost converter with RLD and RCD snubber cell, (b) the current and the voltage waveform of the switch in the transition time.

As Fig. 5(a) shows, the RLD or the turn-on circuit includes a diode and resistor with a parallel inductor in series to the switch device. Whereas, RCD or turn-off circuit includes a parallel resistor and diode in series with a capacitor. The capacitor C and the inductor L delay the time at which the switch reaches the final value of voltage and current. In return, the values of the capacitor and the inductor are usually optimized in

order to minimize the power dissipated in the switch. However, it may not be the best value of the snubber elements from the reliability point of view. The stress in the switch is reduced but the losses persist. Therefore, in the proposed snubber circuit, the elements are selected based on maximum reliability considerations for the set of the switch and its snubber [20]. As a result, it ensures soft-switching and a minimal power loss for the switch. As shown in Fig. 5(b), in this circuit when the switch starts turning off, load current charges the capacitor C up to the source voltage V. Consequently, it delays the time at which the capacitor (also switch) voltage waveform reaches the final value V, the snubber capacitor allows the voltage to rise and reach full value V after the switch current falls to zero. Besides, the same scenario is achieved by the snubber inductor that allows the current to rise and reach full value I after the switch voltage falls to zero.

4.2. Operating Mode of the Circuit

Assuming that the capacitors and the inductors in the circuit are lossless, all diodes are ideal and the initial conditions are regarded. The converter operates under switching period T_s with a duty cycle D in four distinct modes, detailed as follows:

First stage $[t_0 < t < t_1]$: at t_1, switch is turned on, and the current I_d has reached 0, thus, as shown in figure, D and D_{s-on} is off, L, L_s, R_{s-off}, C_s and the MOSFET are on. The current in the main inductor L is given by:

$$i_L(t) = i_L(t_0) + \frac{V_{in}}{L + L_s}(t - t_0), \tag{5}$$

$$i_K(t) = i_L(t) + i_{R_{s-off}}(t). \tag{6}$$

In addition,

$$i_{R_{s-off}}(t) = \frac{V_{out}}{R_{s-off}} e^{-\frac{t}{\zeta}}, \tag{7}$$

where $\zeta = R_{s-off}C_s$ is the time constant.

This mode is ended when the snubber capacitor C_s is dissipated in the resistor R_s. The capacitor C_s is completely discharged in a set duration of $\Delta t_1 = 5\zeta$. Thus, $t_1 = \Delta t_1 + t_0$ and $V_{C_s}(t_1) = 0$.

Second stage $[t_1 < t < t_2]$: in $t = t_1$, as seen in the figure, the voltage across the capacitor reaches the zero, also $V_k(t) = 0$ and $V_{R_{s-off}}(t) = 0$. Therefore:

$$i_k(t) = i_L(t) = i_L(t_1) + \frac{V_{in}}{L + L_s}(t - t_1). \tag{8}$$

At $t = t_2$, the switch is turned off. Thus, $t_2 = t_1 + t_{on}$.

Third stage $[t_2 < t < t_3]$: at $t = t_2$, the capacitor C_s starts to charge while the switch is always off and the diode in the circuit turn-off is on. In this case, the resistor R_{s-off} does not take part in the circuit. Hence, the switch voltage is given as:

$$V_k(t) = V_{cs}(t), \tag{9}$$

$$V_k(t) = V_{in}(1 - \cos(\omega_0(t - t_2))) + \\ + \frac{i_L(t_2)}{C_s\omega_0}\sin(\omega_0(t - t_2)), \tag{10}$$

where $i_L(t_2)$ is the initial value of the inductor current i_L. And:

$$\omega_0 = \frac{1}{\sqrt{(L + L_s)C_s}}. \tag{11}$$

At $t = t_3$ $i_k(t) = 0$, $V_{R_s}(t) = 0$, and the inductor voltage declines from V_{in} to $V_{out} - V_{in}$. In this case, the stage ends whenever the voltage above the capacitor C_s reaches the output voltage V_{out}.

Fourth stage $[t_3 < t < t_4]$: in this stage, the switch remains off, while the diode of the converter D starts conducting, the Photovoltaic panel (PV) generator will be connected directly to the load. At $t = t_4$, the stage ends and the cycle gets repeated again by turning on the switch. Therefore, $t = t_4 = t_2 + t_{off}$ and $t_4 = t_0$.

4.3. Design Procedure of the DC-DC Boost Converter Employing with the Passive Snubber

The proposed snubber circuit for the solar DC-DC boost converter contains the conventional boost circuit elements L, C_{out}, R_{load}, D and the MOSFET with the RLD and RCD circuit. The mean expression of the circuit components is explained in the following subsections:

Boost's Inductor L: the value of the inductor L should be well designed in order to lower the amount of ripple in the main inductor current Δi_L. Therefore, the parameter value of L for desired current ripple is given by [19]:

$$L \geq \frac{V_{in}(1 - D)}{f_{sw}\Delta i_L}, \tag{12}$$

where: Δi_L is the current ripple with $\frac{\Delta i_L}{i_L} \leq 10$ %; f_{sw} is the switching frequency used in the converter; V_{in} is the input voltage; D is the duty cycle.

Boost's output Capacitor C_{out}: the output capacitor controls the ripple produced in the load voltage V_{out}. It is designed as follows [8]:

$$C_{out} \geq \frac{I_{out}D}{f_{sw}\Delta V_{out}}, \tag{13}$$

where ΔV_{out} is the voltage ripple with $\frac{\Delta V_{out}}{V_{out}} \leq 5$ %.

Snubber's Inductor L_s: during the rise time t_r, the rate rises of the switch current defined by $\frac{I_{in}}{t_r}$.

The value of the inductor should be designed to limit the high value of $\frac{di}{dt}$ of the switch device [20]. Thus by:

$$\frac{V_s t_r}{I_{in}} < L_s. \tag{14}$$

Snubber's Resistor R_{s-off}: this resistor represents the very critical element in the circuit, so the design mistake can heat the device or may damage the circuit. As a minimum value, the resistor should assure that the total flowing current across the switch should not overpass the peak repetitive current I_{rpk} of the switch device. During the turn on, C_s has to discharge the current in the minimum time specified by the constructor, otherwise the excess amount of current will pass into the switch. Then, the value of the resistor is given by [19]:

$$\frac{V_{out}}{I_{rpk} - I_{in} - I_{rr_{diode}}} < R_{s-off} < \frac{t_{on\ \text{of the device}}}{5C_s}, \tag{15}$$

where: $I_{rr_{diode}}$ is the diode current during the recovery period; I_{rpk} is the reverse peak current.

5. Results and Discussion

5.1. Simulation Results

In order to validate the impact of passive snubber on the circuit, a simulation model is proposed in the environment of Pspice OrCAD, using the same switches reference chosen for the implementation of the Boost converter: the STW45NM50 MOSFET and the BYT30P diode from the STMicroelectronics, as shown in Fig. 6.

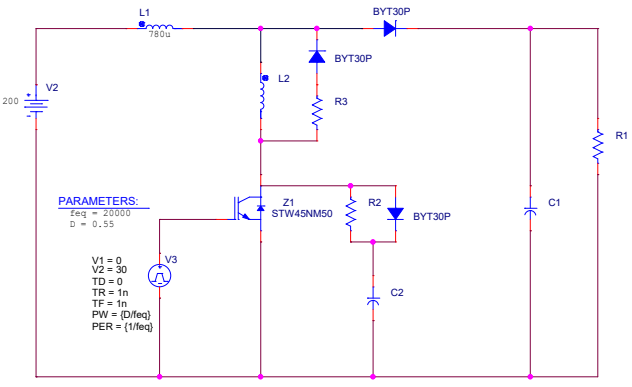
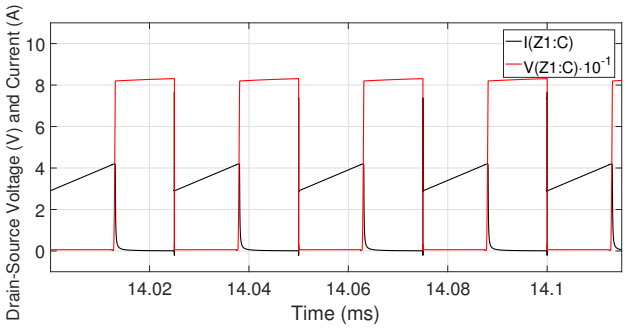
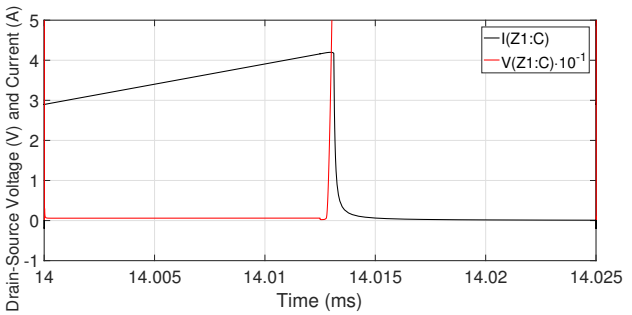


Fig. 6: Pspice model of soft-switching DC-DC boost converter.

The model operates in the conduction current mode at the frequency of 20 kHz, and it adopts the MPPT control algorithm to extract the maximum power from photovoltaic panel arrays. Besides, the voltage waveforms in the following simulation figures are reduced by a coefficient of 10 to have the same magnitude as the current.

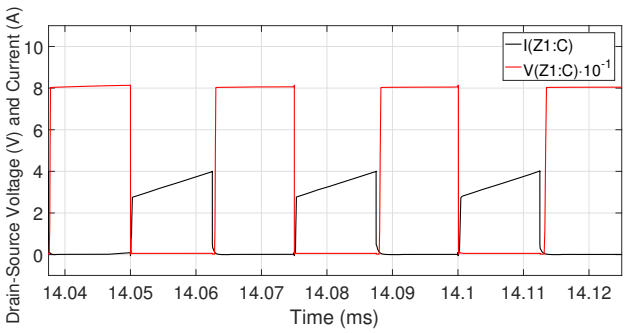


(a) Voltage and current waveform.

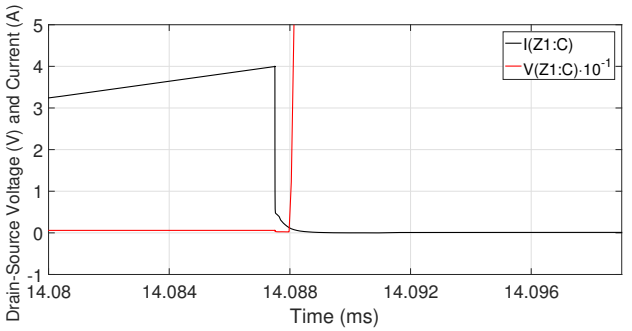


(b) The turn-off moment.

Fig. 7: The waveform in the active switch for the hard-switching, (a) voltage and current in the switch for the conventional circuit, (b) zoom in on the turn-off moment for the switch.



(a) Current and voltage waveform.

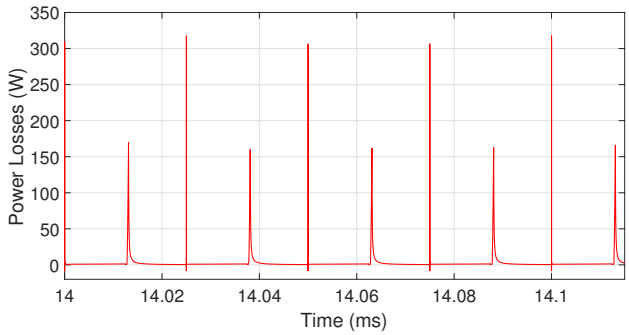


(b) The turn-off moment.

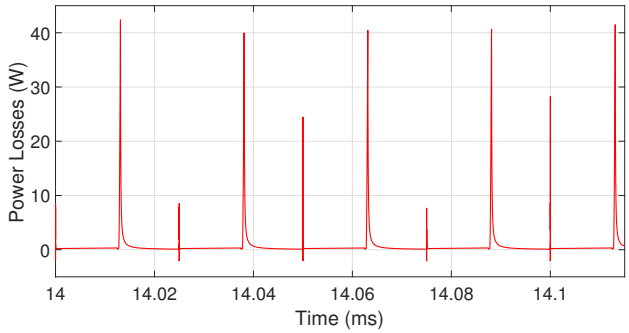
Fig. 8: The waveforms for the active switch in the soft-switching operating mode, (a) voltage and current in the switch for the proposed circuit, (b) zoom in on the turning-off moment in the switch.

Figure 7 presents the switch waveforms of a conventional boost converter operated in the hard-switching condition. In this case, the turn-off processes of the device attained high voltage and current values. And, that is linked to the fast changes of the voltage $\frac{dv}{dt}$. The proposed circuit achieved a soft-switching with a zero voltage switch at turn-off. Due to the control of R_s, C_s improved the performance significantly by reducing the changing rate $\frac{dv}{dt}$, which raised the switch's voltage gradually from 0 to V_0, as shown in Fig. 8.

On this ground, the switching loss of the proposed advanced circuit gets reduced to a lower loss compared to the one in the conventional boost converter with hard-switching operating mode, owing to the deduction of the $\frac{dv}{dt}$ and $\frac{di}{dt}$. As Fig. 9 shows, the lessen losses reach 65.55 % in the switch.



(a) Hard-switching power losses.



(b) Soft-switching power losses.

Fig. 9: Power losses in the switch: (a) hard-switching operating mode, (b) soft-switching operating mode.

5.2. Hardware Implementation Results

The performance characteristics of both the conventional and the proposed boost converters are verified by the prototype of 1.6 kW and 20 kHz switching operation using the same components and the same conditions as the model studied in the simulation environment. The prototype itself is summarized in the appendix, with the aforementioned design considerations. The converter operated with a source simulating photovoltaic panel (PV) as a source.

The signal gate is given to the devices through an intermediate interference circuit that provides isolation from the hardware power circuit and the control circuit, as shown in Fig. 10. This circuit integrates a 6N137 optocoupler for insulation, and an IR2112 driver, which amplifies output signals delivered by the control card from low voltage 3.3 V to reach the minimum gate threshold voltage of the MOSFET, which corresponds to 15 V.

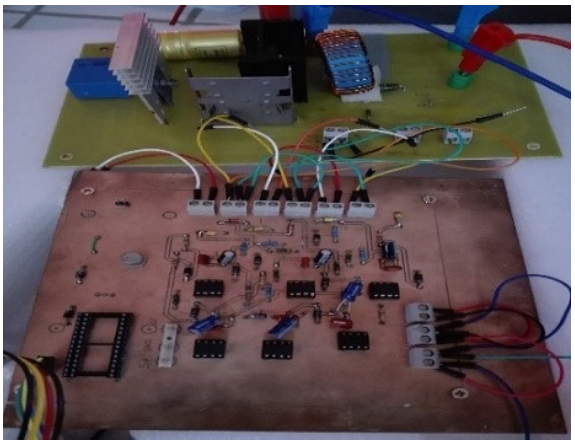


Fig. 10: Hardware set-up of the boost converter with the galvanic-isolation circuit.

In the proposed implementation, we tested our prototype using a low power supply. As illustrated in Fig. 11, the voltage in the conventional circuit presents a high voltage spike between the drain and the source during device turn-off. It exceeds the rating of the switch device.

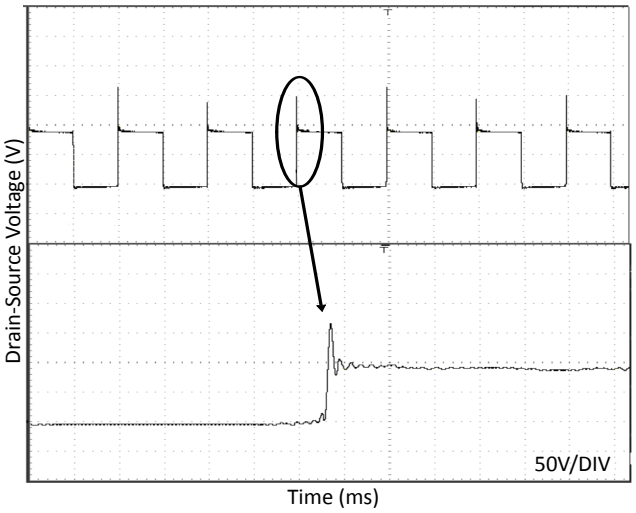


Fig. 11: Voltage waveform of the conventional boost's switch in hard-switching.

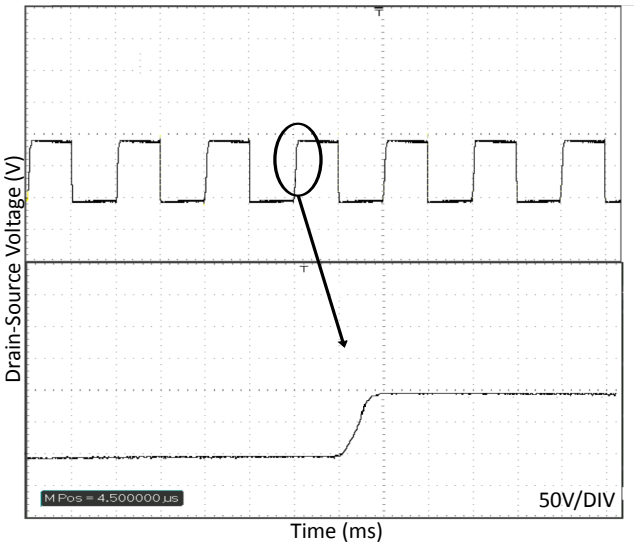
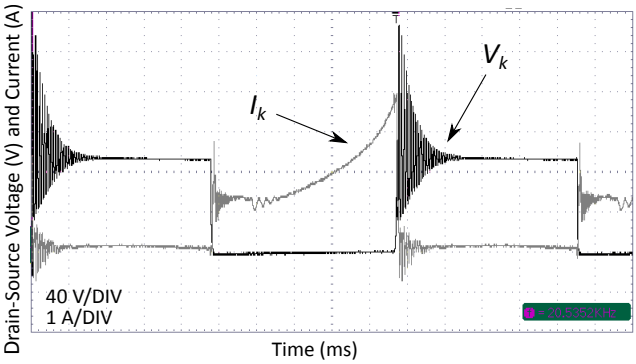
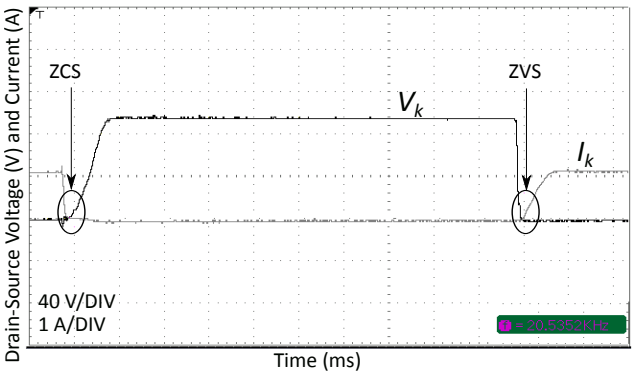


Fig. 12: Voltage waveform V_k of the proposed boost's switch in soft-switching.



(a) Hard-switching operating mode.

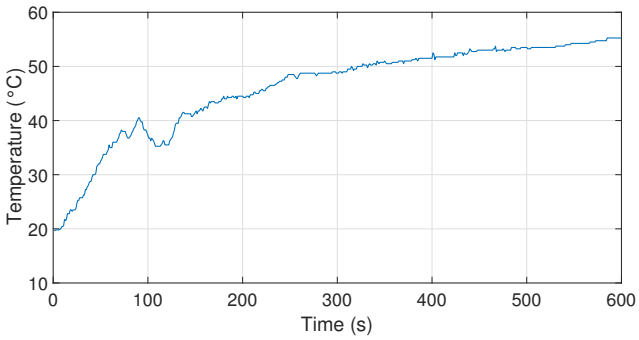


(b) Soft-switching operating mode.

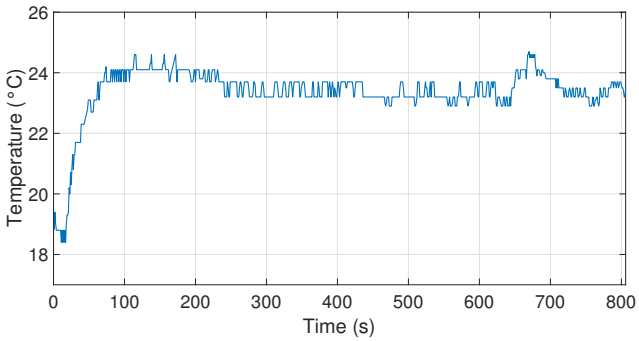
Fig. 13: Comparison of voltage and current waveform for the boost's MOSFET for the (a) conventional converter and (b) proposed model.

The proposed circuit with a passive snubber has shown a better waveform of the voltage by eliminating the high spike voltage and reducing the fast-changing rates, as visualized in Fig. 12. The voltage and the current in Fig. 13(a) and Fig. 13(b), in both conventional and the proposed converter, verify the theoretical waveform. Due to the resonant circuit, RLD and RCD provide a retard for the current and voltage increases by raising the changing rate $\frac{di}{dt}$ and $\frac{dv}{dt}$, respectively. The MOSFET in the proposed circuit had zero switching point at the turn-off and turn-on. Consequently, it exhibits zero power losses during turn-on and turn-off.

The junction temperature is one of the most important parameters that influence the performance and the behavior of the MOSFET. Thus, to provide a realistic visualization of the temperature dynamic behavior for the conventional boost and proposed circuit, an LM35 temperature sensor was implemented into the switch device.



(a) Hard-switching operating mode.



(b) Soft-switching operating mode.

Fig. 14: The MOSFET junction temperatures measured for the conventional boost and the proposed boost, (a) hard-switching operating mode, (b) soft-switching operating mode.

From Fig. 14(a), it can be observed that hard-switching mode operating increases the temperature in the MOSFET up to 58 °C due to the presence of the spikes, ripples as was seen in Fig. 13(a), and the high-power losses, which impact the performance of the switch and contribute to accelerated aging of the device. Comparing to that, the proposed circuit has shown a better dynamic behavior of the temperature by reducing it into 44.44 %, as given in Fig. 14(b), owing to the fewer power losses and the good waveforms of the voltage and current above the switch.

6. Conclusions

This paper points out the comparison between hard-switching and soft-switching for a solar DC-DC boost converter. The soft-switching is based on a passive snubber RLD and RCD circuits. The operation principals and the design consideration of the proposed circuit have been described on the basis of the theoretical and experimental points of view. It was observed that the soft-switching enhances the circuit's waveform, by reducing the stress on the switch and hence lessening the power losses in the converter into 65.55 %. Moreover, the junction temperature is reduced by 44.45 %. It keeps it stable at a nominal temperature area of the MOSFET. On that ground, analytically and experimentally, it was found that the conventional boost converter circuit achieves better efficiency when the passive snubber circuit is implemented compared to the hard-switching operating mode.

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Appendix A

Tab. 1: Boost Converter Parameters.

Parameter	Specification
Input voltage	200 V
Output voltage	400 V
Output power	1.6 kW
Maximum output current	4 A
Switching frequency	20 kHz
Filter inductor	700 µH
Output filter capacitor	100 µF
Diode	BYT30P
Active switch	MOSFET STW45NM50