RESOURCES OF DIGITAL FIR FILTERS HARDWARE IMPLEMENTATION IN FPGAs FOR DIGITAL IMAGE PROCESSING IN REAL TIME

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Summary The main image information content, from the human visual system viewing point, is focused into whole colorimetric and spatial information. Because every image is result of some previous processes, the goal for all standard image processing methods is improvement colorimetric and spatial image parameters in relation maximum information content by the complicated and expensive systems for digital image processing in (quasi)real time [1] based on the flash signal (multi)processors. Some single-purpose applications do not need the robust and flash systems for DIP and be enough for their use single digital filters with suitable hardware implementation. In the contribution discussed problem is therefore focused on the short description of FIR digital filters and their hardware implementation in FPGAs-Xilinx for usage in the image processing in real time include obtained experimental results.

1. ONE-DIMENSIONAL DIGITAL FIR FILTER DEFINITION AND DESCRIPTION

Let we have m - bit (e.g. 8bit) data array $\{pin_{R,G,B,Y}(k,l)\}_{k,l=1}^{K,L}$ or long data vector $\{pin_{R,G,B,Y}(w)\}_{w=1}^{K.L}$ as math representation of some digital 2D mono-chrome/component colour image, which is result of scanning and digitalisation process an original analogue colour image $pin(x,y,\lambda)$. Then digital FIR filter for image processing in real time may be defined as linear causal and in time invariant system of order N_0 with followed transfer function $H_{FIR}(z)$ in complex z - plane

$$H_{FIR}(z) = \beta_0 + \beta_1 z^{-1} + ... + \beta_{N_0} z^{-N_0} \quad (1)$$

and the output response

$$pout_{R,G,B,Y}[k,l] = \sum_{r=0}^{N_0} \beta_r pin_{R,G,B,Y}[k-r,l], \ \ldots \ \forall k,l \quad (2)$$

or

$$pout_{R,G,B,Y}[k,l] = \sum_{r=0}^{N_0} pin_{R,G,B,Y}[k-r,l] h_{FIR}[r], \ \ldots \ \forall k,l \quad (3)$$

or

$$pout_{R,G,B,Y}[w] = \sum_{r=0}^{N_0} pin_{R,G,B,Y}[w-r] h_{FIR}[r], \ \ldots \ \forall w \quad (4)$$

where $\{h_{FIR}[r]\}_{r=0}^{N_0} = \{\beta_r\}_{r=0}^{N_0}$ is its finite impulse response. Because digitalisation process of analogue colour image $pin(x,y,\lambda)$ is usually realised with its (video-) signal representation $pin_{R,G,B,Y}(t)$, then for selected sample frequency $f_{sa} = \frac{1}{t_{sa}} = K.f_H = K.L.f_{vp}$ and substitution $z = e^{j2\pi f t_{sa}} = e^{j2\pi \frac{f}{f_{sa}}} = e^{j\Theta}$ in frequency domain can be defined complex transfer function $H_{FIR}(e^{j\Theta}) = H_{FIR}(j\Theta)$ of digital FIR filter in following state

$$H_{FIR}(j\Theta) = \sum_{r=0}^{N_0} h_{FIR}[r] e^{-jr\Theta} = M_{FIR}(\Theta) e^{j\Phi_{FIR}(\Theta)} \quad (5)$$

where $M_{FIR}(\Theta)$ is its module frequency characteristic and $\Phi_{FIR}(\Theta)$ is its phase frequency characteristic. The special case of digital filters are I-FIR filters with symmetrical impulse response

$$h_{FIR}[r] = h_{FIR}[N_0 - r] = h_{FIR}[2M_0 - r], \ \ldots \forall r=0,1,\ldots, N_0 \quad (6)$$

when AFCH is symmetrical and periodical with period 2π

$$M_{FIR}(\Theta) = h_{FIR}[M_0] + 2\sum_{r=0}^{M_0-1} h_{FIR}[r]\cos[\Theta(M_0 - r)] \quad (7)$$

and PFCH is linear

$$\Phi_{FIR}(\Theta) = -M_0\Theta . \quad (8)$$

2. ONE-DIMENSIONAL DIGITAL FIR FILTER STANDARD HARDWARE IMPLEMENTATION

Whatever hardware implementation of some system presumes his concrete suitable inside structure. For the case of 1D digital I-FIR filters hardware implementation the simplest suitable inside structure, known as transversal non-recursive structure, is by Eq.(1) shown in Fig.1.

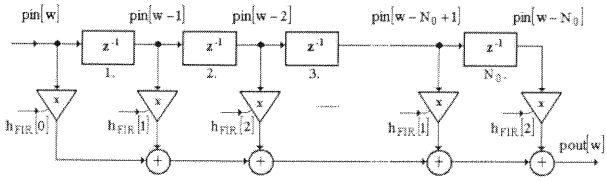

Fig.1. Transversal non-recursive inside structure of digital I-FIR filter of order $N_0 = 2M_0$.

The circuit realisation of separate functional blocks (retarders, multipliers and adders) is from one side coupled onto disposition programmable device (e.g. FPGA) and its development software, and from second side is coupled onto processed video-signal distribution form (parallel or serial).

2.1. Retarders of fir filter hardware implementation in fpga xilinx for 8bit parallel distributed arithmetic

From Eq.(1)÷(4) and Fig.1 results, that retarders connected in cascade generate time delayed image samples sequence $pin(w), pin(w-1), \ldots, pin(w-N_0)$ needed for output image sample $pout(w)$ calculus and may be implemented as shift data register with parallel distributed data. Separate retarder (z^{-1}) then can be implemented as 8bit parallel data register by usage

LogiBLOX generator (see Fig.2) or New Symbol Wizard generator.

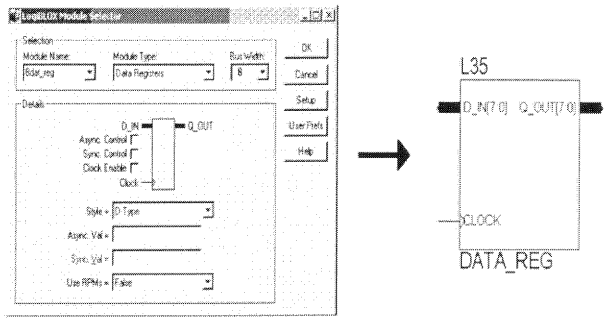

Fig. 2. Separate retarder hardware implementation in FPGA Xilinx.

2.2. Multipliers of fir filter hardware implementation in fpga xilinx for 8bit parallel distributed arithmetic

For expected bit representation width of impulse response samples $h_{FIR}[r]$, e.g. 3bit, the separate multipliers in Fig.1 can be implemented as 8bit x 3bit parallel multiplier with 8bit + 3bit width of output product by usage New Symbol Wizard (NSW) generator. In Fig.3 is shown example of this implementation for the case of multiplier with registered output and inside structure which responds to standard algorithm of arithmetic product operation.

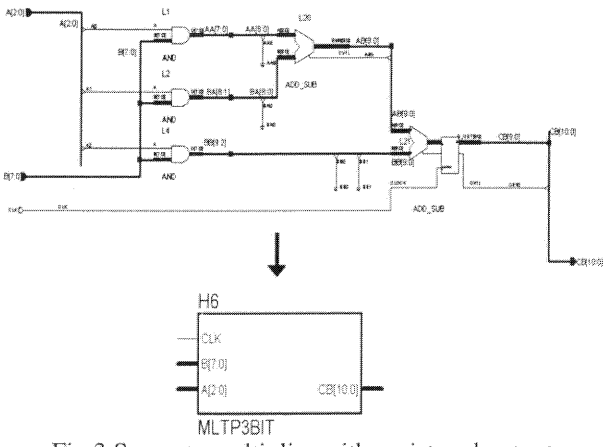

Fig.3 Separate multiplier with registered output hardware implementation in FPGA Xilinx

2.3. Adders of fir filter hardware implementation in fpga xilinx for 8bit parallel distributed arithmetic

Because by Fig.1 all separate adders are working with (8+3) bit products, with some reserve can be implemented as (11+reserve) bit parallel adders/ subtracters by usage LogiBLOX generator (see Fig.4). The control input Add/Sub in this selection may be used for sign of an impulse response samples $h_{FIR}[r]$ realisation.

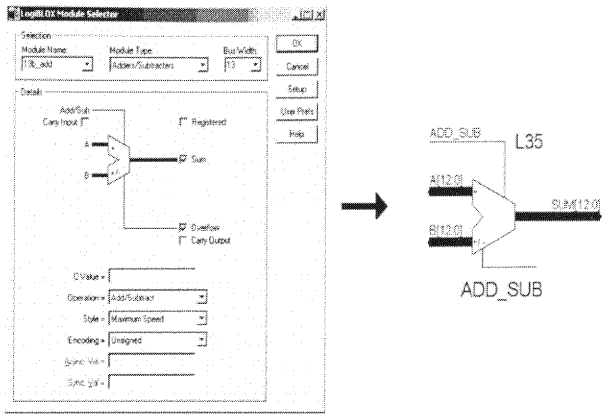

Fig. 4. Separate adder hardware implementation in FPGA Xilinx.

3. THE EXAMPLE OF I-FIR FILTER STANDARD HARDWARE IMPLEMENTATION AS 1D EDGE DETECTOR

One of many 1D edge detectors realisation can be interpreted as following 5th order I-FIR filter impulse response definition

$$\begin{matrix} h_{FIR}[0] & h_{FIR}[1] & h_{FIR}[2] & h_{FIR}[1] & h_{FIR}[0] \\ -1 & -1 & 4 & -1 & -1 \end{matrix} \quad (9)$$

with hardware implementation in FPGA Xilinx – XC4010EPC84 shown in Fig.5a and time verification shown in Fig.6.

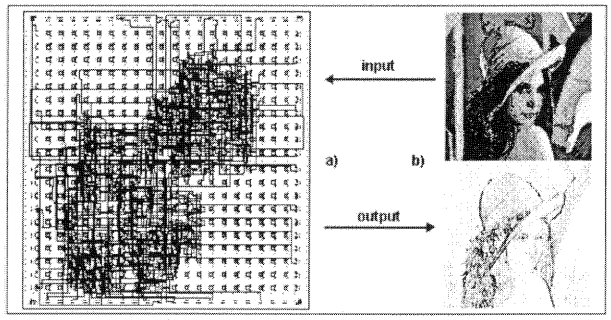

Fig..5. The example of I-FIR filter hardware implementation as 1D edge detector.

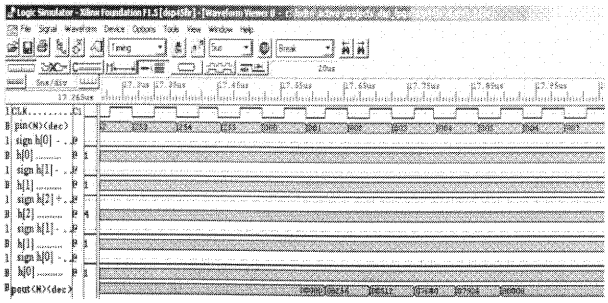

Fig. 6. Time verification of I-FIR filter hardware implementation as 1D edge detector.

4. ONE-DIMENSIONAL DIGITAL FIR FILTER HARDWARE IMPLEMENTATION BY OTHER METHOD

The another approach to hardware digital FIR filter implementation is usage NSW generator by Fig.7 with connection a VHDL editor for inside structure editing. Example of universal inside structure for 5th order FIR

filter represented by VHDL source code is shown in the next comprehensive listing - Fig.8.

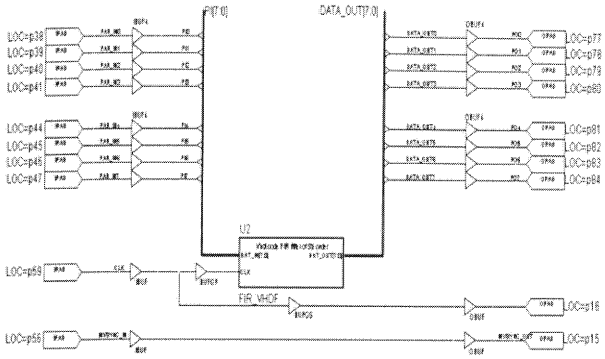

Fig. 7. Non-recursive transversal digital I-FIR filter hardware implementation by NSW generator.

```
entity FIR_VHDC is
port (
In_dat:  in BYTE;
CLK:     in STD_LOGIC;
Out_dat: out BYTE
);
end FIR_VHDC;

architecture FIR_VHDC_arch of FIR_VHDC is
SIGNAL tap  : ARRAY_BYTE;   -- Tapped delay line
of bytes
SIGNAL IBUF : DBYTE;
begin

p1: PROCESS          ------> Behavioral Style
BEGIN
WAIT UNTIL CLK='1';
-- Compute output Out_dat the filter coefficients weight
   for 5th order FIR
-- The coefficients are [ h(0) h(1) h(2) h(3) h(4)]
-- IBUF <= +-h(2)*tap(2)+-h(0)*tap(0)+-h(1)*tap(1)+-
   h(3)tap(3)+-h(4)*tap(4); ----> universal pattern

--  IBUF <= tap(2); ----- > grabbing  (1st version)
    IBUF <= 3*tap(2) - tap(1) - tap(3) ; ------- > 2nd
    order PreM phassis (2nd version)

if (IBUF <= -1) then
Out_dat <= 0;
elsif (IBUF >= 256) then
Out_dat <= 255;
else
Out_dat <= IBUF;
end if;

FOR I IN 4 DOWNTO 1 LOOP
tap(I) <= tap(I-1); -- Tapped delay line: shift one
END LOOP;
tap(0) <= In_dat;
END PROCESS;

end FIR  VHDC  arch;
```

Fig. 8. Example of universal inside structure for 5th order FIR filter represented by VHDL source code.

5. SOME OBTAINED EXPERIMENTAL RESULTS

All for this time experimental tests with hardware implementation of FIR filtres was been realised with experimental CPLD/FPGA development board ET101, [2]. This hardware equipment have been extended by the peripheral A/D and D/A modules which are working with sample frequency ≈ 14.75 MHz and are based with Analog Devices products. Full view on to extended board ET101 is shown in Fig.9. On the next figures – Fig.10 ÷ Fig.12 are presented Basic Image Processing Operations (BIPO)

- image grabbing
- image smoothing
- image edges detecting

in real time realised by the FIR digital filters hardware implemented in FPGA - XC 4000 series (in XC4006E and XC4010E).

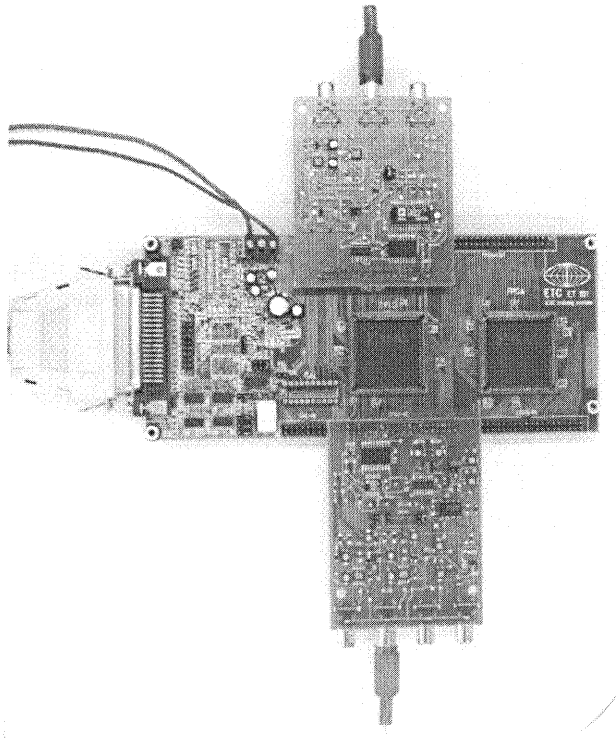

Fig. 9. Extended experimental development board for digital I-FIR filter hardware implementation.

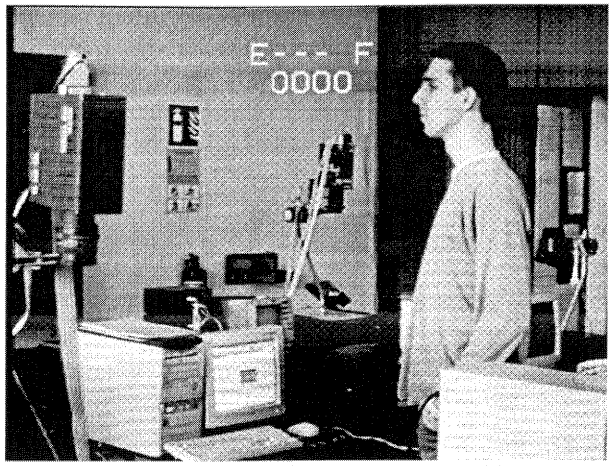

Fig. 10. BIPO in real time – image grabbing.

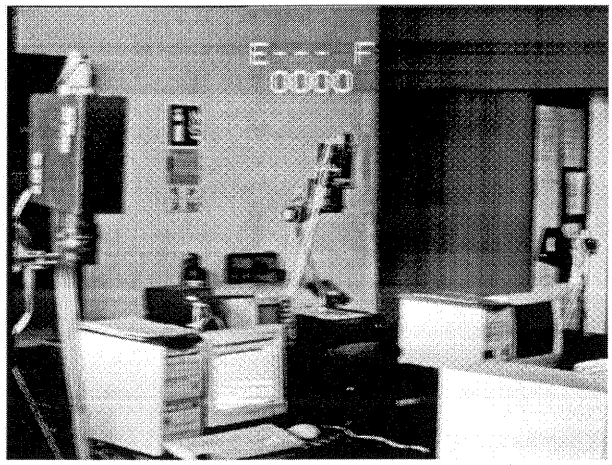

Fig. 11. BIPO in real time – image smoothing.

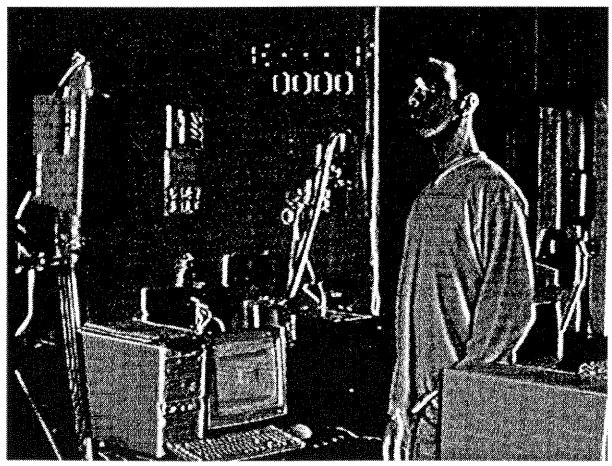

Fig. 12. BIPO in real time – image edges detection .

6. CONCLUSION

In summary we have interested of two resources of digital FIR filters hardware implementation in Field Pragrammable Gate Arrays. One of them can be classified as standard advance when in the development process are used standard blocks from the Xilinx library and LogiBLOX generator. The second one can be classified as non – standard, but very modern advance, when in the development process is used New Symbol Wizard generator and the HDL platform for FIR filters description.

Very positive obtained result for us was been fact, that in the FPGA implemented digital filters working in real time with any videosignals, generated by CCIR video sources, e.g. CCD cameras, recorders, etc.

In our opinion the described results find exploitation not only in the university education process, but in the special technical applications, too.

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