A Class of Differentiator-Based Multifunction Biquad Filters Using OTRAs

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Abstract. *This paper presents Signal Flow Graph (SFG) approach-based realization of Single Input Multiple Output (SIMO) filter topologies. A differentiator is placed as basic building block. A total of sixteen variants are derived from the proposed differentiator-based SFG. The Operational Trans-Resistance Amplifier (OTRA), an active block having low parasitics at input terminals, is used to validate the proposed methodology. All the derived filter structures use three OTRAs, six resistors and two capacitors. The filter performance parameters can be adjusted independently. The functional verification of the proposed method is done via SPICE simulations using 0.18 μm CMOS technology parameters from MOSIS.*

Keywords

Filter, OTRA, SIMO.

1. Introduction

The Continuous-Time (CT) filters are widely used in consumer electronics, instrumentation, military ordnance, telecommunications and radar systems, etc. Therefore, considerable research efforts have been devoted to developing CT filters based on wide variety of active blocks. The bandwidth of traditional active blocks is limited by closed-loop voltage gain and presence of the parasitic elements influences the performance of filter. The active block, OTRA [1], uses current feedback technique, which makes its bandwidth almost independent of the gain. Additionally, the parasitic impedances at input terminals are low and have negligible effect on circuits. Therefore, OTRA-based CT filters have been investigated in recent past [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18] and [19] and they can be categorized as (i) single and (ii) multiple OTRA-based structures. Though single OTRA-based filters [2], [3], [4] and [5] are useful when power consumption is important, they show larger sensitivity to component variation and are less versatile than their multiple OTRA-based counterparts [1], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18] and [19]. The salient features of the available multiple OTRA-based CT filters are listed below:

- A single response is available in [1], [6], [7], [8], [10], [16] and [17], whereas [8], [9], [11], [12], [13], [14] and [15] offer multiple responses.

- Single/Multiple output filters [6], [7], [8] and [16] may, however, give other responses by choosing appropriate input excitation terminal.

- Filters [1], [8], [10], [16] and [18] impose condition on component/switch selection for obtaining the responses.

The underlying principle of these filters [1], [6], [10], [11], [12], [13], [14] and [16] is connection of lossy and lossless integrator. In the recent past, the researchers have developed few differentiator-based signal processing and generating circuits [7], [8], [9], [15], [20], [21], [22], [23], [24], [25], [26], [27] and [28] finding applications in the area of control system and biomedical instrumentation. However, the area is not much explored, as evident from the limited literature available. Considering this, differentiator-based SIMO filter topologies designed using SFG-based approach are proposed in this paper and OTRA is used to validate it.

It is pertinent to mention here that SFG-based approach, with integrators, has been employed in [29], [30], [31], [32] and [33].

The paper is arranged in five sections. Section 2. includes the discussion on the proposed SFG, followed by a brief review of OTRA and basic signal processing blocks designed using OTRA. The OTRA-based SIMO filter topologies are also included in the same section subsequently. The non-ideality analysis is given in Sec. 3. , followed by simulation results in Sec. 4. The paper is finally concluded in Sec. 5.

2. Circuit Description

2.1. The Proposed SFG

The proposed differentiator-based SFG, which uses two differentiators in forward path, is depicted in Fig. 1. The coefficients k_i ($i \in \{1, 2, 3, 4\}$) may assume value 1 and -1. Four different SFGs can be generated from Fig. 1 by selecting the values of k_1 and k_2 respectively as $(1,1)$, $(1,-1)$, $(-1,1)$ or $(-1,-1)$ as depicted in Fig. 2. These SFGs represent four different topologies and are referred respectively as topology 1, topology 2, topology 3 and topology 4. The values of k_3 and k_4 are chosen so that appropriate transfer functions can be obtained.
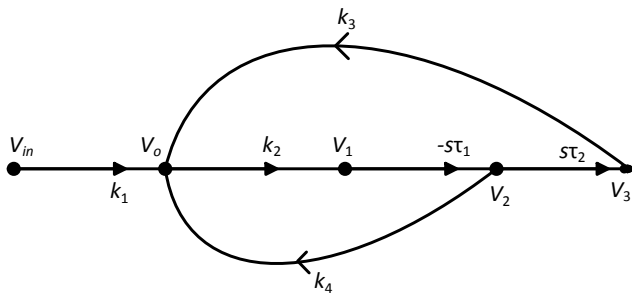

Fig. 1: The proposed differentiator-based SFG.

It may be noted that the SFG in Fig. 1 uses an inverting differentiator, followed by a non-inverting differentiator. Alternate SFGs can be derived by placing

- a non-inverting differentiator followed by an inverting differentiator,

- two non-inverting differentiators, or

- two inverting differentiators.

The resulting SFGs are depicted in Fig. 3.

In each SFG in Fig. 3, k_1 and k_2 may further be selected as $(1,1)$, $(1,-1)$, $(-1,1)$ or $(-1,-1)$, thus providing a total to sixteen SFGs, and are shown in Fig. 4.
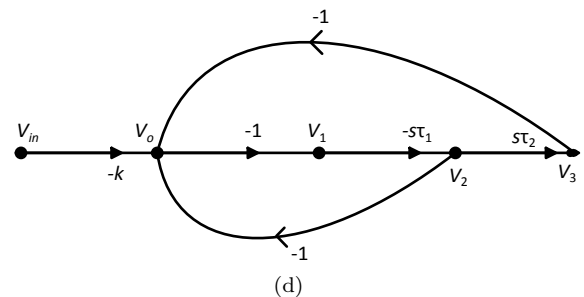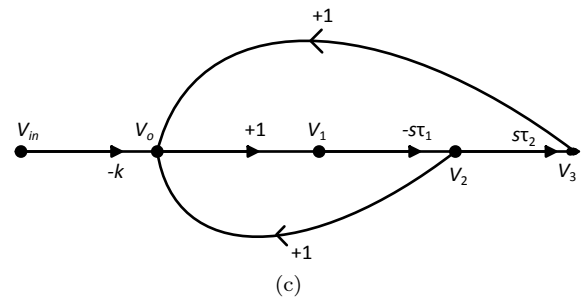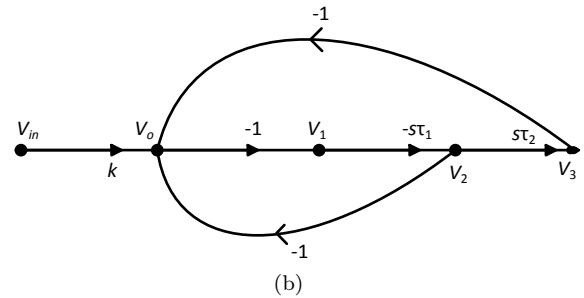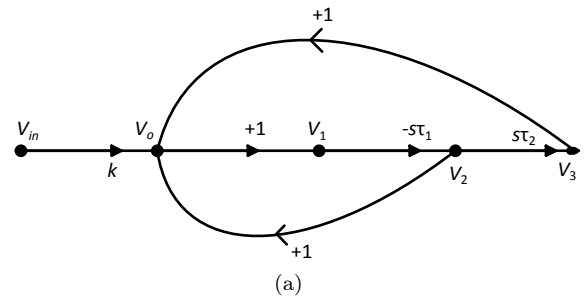

Fig. 2: SFGs generated from Fig. 1 for k_1 and k_2 as (a) topology 1, (b) topology 2, (c) topology 3, (d) topology 4.

2.2. The OTRA

The OTRA is an active block with two low-impedance input terminals and a low-impedance output terminal. The circuit symbol of OTRA is given in Fig. 5 and its terminals are characterized by matrix of Eq. (1):

$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \cdot \begin{bmatrix} I_p \\ I_n \\ I_0 \end{bmatrix}, \qquad (1)$$

where R_m is trans-resistance gain of OTRA. The value of R_m is ideally infinity; therefore, OTRA is generally used in negative feedback configuration.
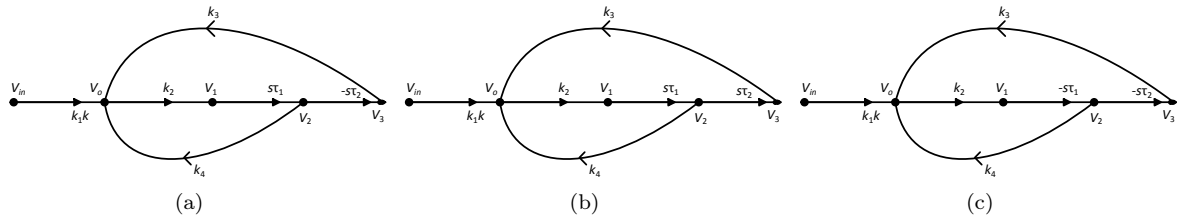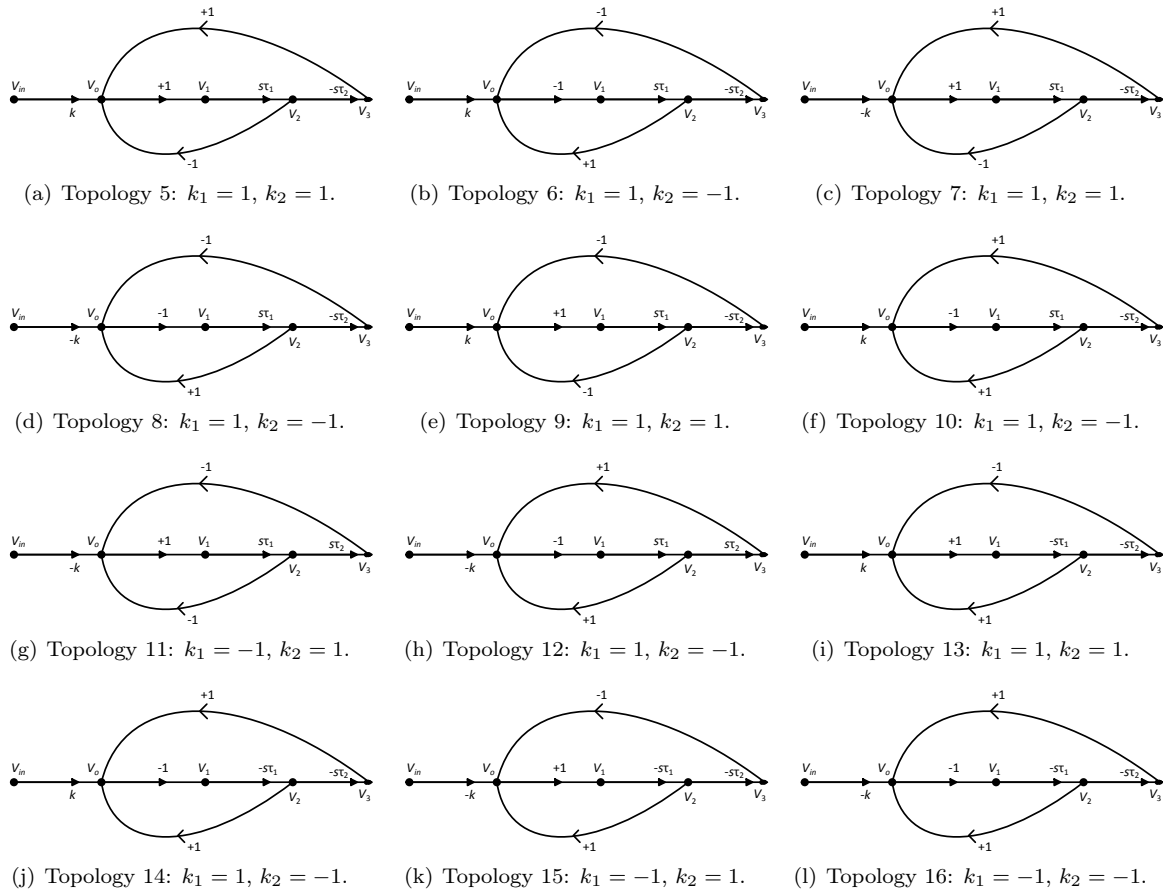
Fig. 3: Alternate SFGs.

(a) Topology 5: $k_1 = 1$, $k_2 = 1$.

(b) Topology 6: $k_1 = 1$, $k_2 = -1$.

(c) Topology 7: $k_1 = 1$, $k_2 = 1$.

(d) Topology 8: $k_1 = 1$, $k_2 = -1$.

(e) Topology 9: $k_1 = 1$, $k_2 = 1$.

(f) Topology 10: $k_1 = 1$, $k_2 = -1$.

(g) Topology 11: $k_1 = -1$, $k_2 = 1$.

(h) Topology 12: $k_1 = 1$, $k_2 = -1$.

(i) Topology 13: $k_1 = 1$, $k_2 = 1$.

(j) Topology 14: $k_1 = 1$, $k_2 = -1$.

(k) Topology 15: $k_1 = -1$, $k_2 = 1$.

(l) Topology 16: $k_1 = -1$, $k_2 = -1$.

Fig. 4: The SFG structures.

Fig. 5: The OTRA block.

The OTRA-based realization of voltage addition/subtraction is shown in Fig. 6. It uses five resistors and one OTRA. By equating the currents of inverting and non-inverting terminals, the output of the circuit from Fig. 6 is obtained as:

$$V_o = R_5 \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} - \frac{V_3}{R_3} - \frac{V_4}{R_4} \right). \qquad (2)$$

Exchanging (V_i, R_i), where $i \in \{1, 2\}$ with (V_j, R_j), where $j \in \{3, 4\}$ in Fig. 6 yields the following relation:

$$V_o = -R_5 \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} - \frac{V_3}{R_3} - \frac{V_4}{R_4} \right). \qquad (3)$$

It may be noted that Eq. (3) is inverting form of Eq. (2).
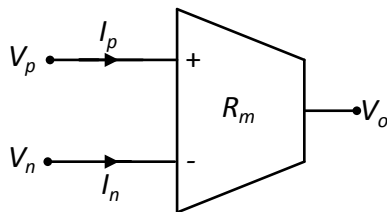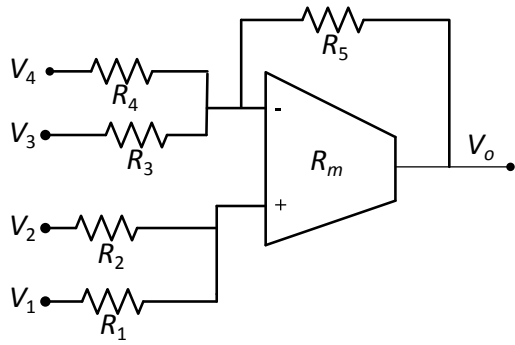
A close inspection of SFGs in Fig. 2 and Fig. 4 reveals that the circuit realization would require voltage addition-subtraction followed by amplifier (inverting / non-inverting), and differentiators (inverting / non-inverting).

Fig. 6: OTRA-based realization of voltage addition/subtraction.

By choosing the values of resistances appropriately, the desired addition-subtraction can be performed. Equation (2) provides non-inverting output, whereas Eq. (3) gives an inverting output.

The OTRA-based circuits of inverting and non-inverting differentiators are given in Fig. 7 and their respective outputs are given by:

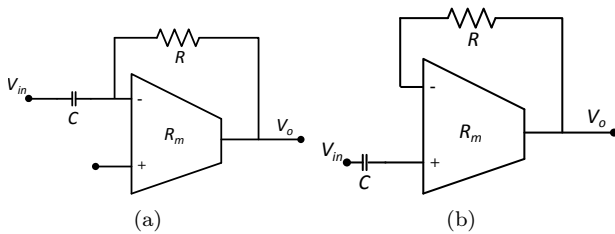$$V_o = -sCRV_{in}, \qquad (4)$$

$$V_o = -sCRV_{in}. \qquad (5)$$

Fig. 7: OTRA-based realization of (a) inverting and (b) non-inverting differentiators.

2.3. OTRA-Based Realization of SFGs

The OTRA-based realization of SFGs can be obtained by using the basic blocks from Fig. 6 and Fig. 7. The corresponding circuit realizations of SFGs from Fig. 2(a), Fig. 2(b), Fig. 2(c) and Fig. 2(d) are depicted respectively in Fig. 8(a), Fig. 8(b), Fig. 8(c) and Fig. 8(d). It may be noted that the realizations from Fig. 8(a) and Fig. 8(b) are same as those given in Fig. 8(c) and Fig. 8(d) respectively, since their corresponding k_1k_2 product terms are the same.
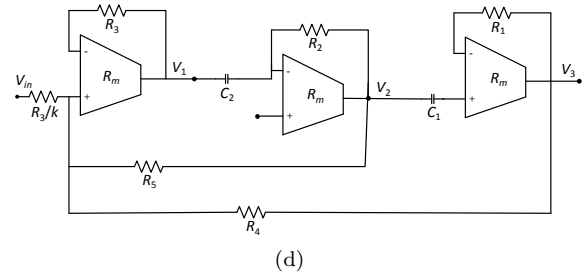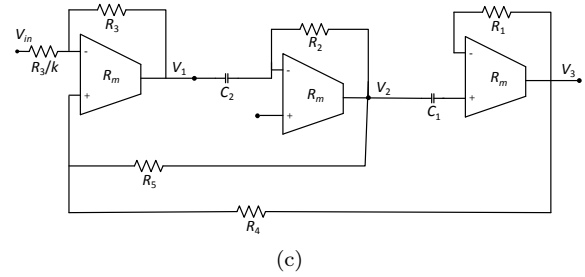

(a)

(b)

(c)

(d)

Fig. 8: OTRA-based realization of SFGs from Fig. 2.
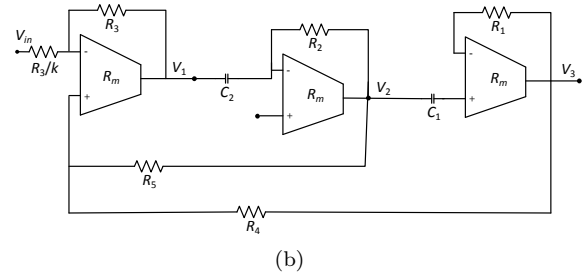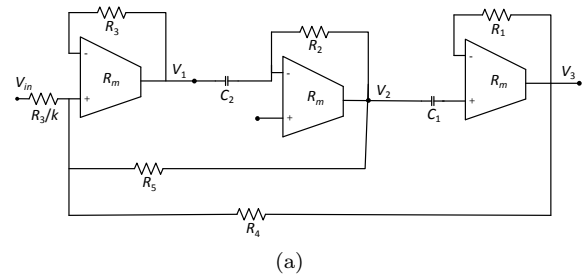
The transfer functions of the topology in Fig. 8(a) are obtained as:

$$\begin{aligned}
\frac{V_1}{V_{in}} &= \frac{k}{D(s)}, \\
\frac{V_2}{V_{in}} &= \frac{-k\left(sR_2C_2\right)}{D(s)}, \\
\frac{V_3}{V_{in}} &= \frac{-k\left(s^2R_1R_2C_1C_2\right)}{D(s)},
\end{aligned} \qquad (6)$$

where

$$D(s) = 1 + \frac{sR_2R_3C_2}{R_5} + \frac{s^2R_1R_2R_3C_1C_2}{R_4}. \qquad (7)$$

The transfer functions of the topology in Fig. 8(b) are computed as:

$$\frac{V_1}{V_{in}} = \frac{-k}{D(s)},$$
$$\frac{V_2}{V_{in}} = \frac{k\,(sR_2C_2)}{D(s)}, \qquad (8)$$
$$\frac{V_3}{V_{in}} = \frac{k\,(s^2R_1R_2C_1C_2)}{D(s)}.$$

It may be noted that V_1, V_2 and V_3 respectively represent low pass, band pass and high pass responses. All the transfer functions at different nodes represented by Eq. (6) and Eq. (8) are characterized by following pole frequency (ω_0), bandwidth ($\frac{\omega_0}{Q}$) and quality factor (Q):

$$\omega_0 = \left(\frac{R_4}{R_1R_2R_3C_1C_2}\right)^{\frac{1}{2}}, \qquad (9)$$

$$\frac{\omega_0}{Q} = \frac{R_4}{R_1R_5C_5}, \qquad (10)$$

$$Q = R_5\left(\frac{R_1C_1}{R_2R_3R_4C_2}\right)^{\frac{1}{2}}. \qquad (11)$$

It is clear from Eq. (9), Eq. (10) and Eq. (11) that both bandwidth and quality factor can be adjusted independently by varying R_5 without modifying the pole frequency. The pole frequency may be varied by changing R_i and C_i ($i = 1, 2$) and quality factor may be kept constant by assuming $R_3 = R_4 = R_5$ and $\frac{R_1}{R_2} = \frac{C_2}{C_1}$. Further, the gain of the filter responses can be changed by varying the value of k.

The OTRA-based realizations of the SFGs listed in Fig. 4 are also obtained and omitted for the sake of brevity. The transfer functions are similar to the one given in Eq. (6), Eq. (7) and Eq. (8).

3. The Non-Ideality Analysis

The response of the filter may deviate due to non-ideality of OTRA. Ideally, the trans-resistance gain R_m is assumed to approach infinity. However, in practice, R_m is a frequency-dependent finite value. Considering a single-pole model for trans-resistance gain, $R_m(s)$ can be expressed as:

$$R_m(s) = \frac{R_0}{1 + \frac{s}{\omega}}, \qquad (12)$$

where R_0 is low-frequency trans-resistance gain. For high-frequency applications, the trans-resistance gain $R_m(s)$ is approximated as:

$$R_m(s) \approx \frac{1}{sC_p}, \qquad (13)$$

where

$$C_p = \frac{1}{R_0\omega_0}. \qquad (14)$$

Taking this effect into account, the transfer functions in Fig. 8(a) in presence of finite transimpedance are computed as:

$$\frac{V_1}{V_{in}}\bigg|_n = \frac{k_n}{D_n(s)},$$
$$\frac{V_2}{V_{in}}\bigg|_n = \frac{-k_n\,(sR_2C_2)}{D_n(s)\,(1 + sR_2C_{p2})}, \qquad (15)$$
$$\frac{V_3}{V_{in}}\bigg|_n = \frac{-k_n\,(s^2R_1R_2C_1C_2)}{D_n(s)\,(1 + sR_2C_{p2})\,(1 + sR_1C_{p3})},$$

where

$$D_n(s) = (1 + sR_3C_{p1}) + \frac{sR_2R_3C_2}{R_5\,(1 + sR_2C_{p2})} + \\ + \frac{s^2R_1R_2R_3C_1C_2}{R_4\,(1 + sR_1C_{p3})\,(1 + sR_2C_{p2})}. \qquad (16)$$

It is clear from Eq. (15) and Eq. (16) that transfer functions modify in presence of non-ideality. These equations reduce to Eq. (6) and Eq. (7) by choosing the operating frequency below $\min\left(\frac{1}{R_3C_{p1}}, \frac{1}{R_2C_{p2}}, \frac{1}{R_1C_{p1}}\right)$.

4. Simulation Results

To verify the proposed scheme, the functionality of the filter from Fig. 8(a) is tested through SPICE simulations using CMOS OTRA architecture of [34] and 0.18 μm CMOS process parameters provided by MOSIS (AGILENT). Supply voltages ±1.5 V are taken. The simulation is performed for pole frequency of 159 kHz and unity quality factor. All the resistances are taken as 10 kΩ and capacitor is taken as 100 pF. The simulated frequency response for low pass, band pass and high pass for the circuit from Fig. 8(a) are depicted in Fig. 9. The total power consumption is found to be 6 mW.

The other set of simulations is carried out to show tuning of band pass filter center frequency and gain. The center frequency is varied by changing R_1 and R_2 simultaneously from 5 kΩ to 20 kΩ in step of 5 kΩ while keeping all other resistances and capacitances at 10 kΩ and 100 pF respectively. This setting leads to constant Q value. Figure 11 shows the simulated band pass response for variation in center frequency and Q with change in resistance. It may be noted that Q varies slightly from unity value, which may be attributed to non-idealities of OTRA.

For variation of band pass response gain while keeping center frequency constant, all resistances except the one connected to input terminal and capacitances are
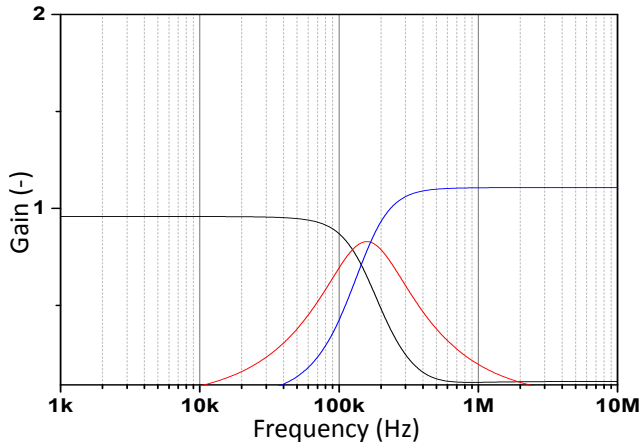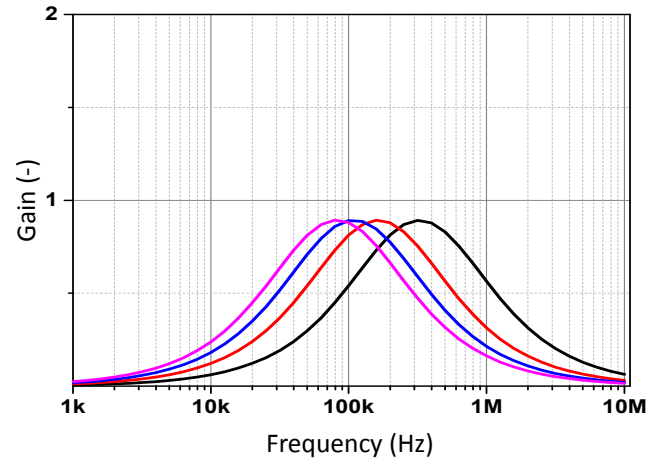
Fig. 9: Simulated low pass, band pass and high pass responses of the circuit from Fig. 8(a).
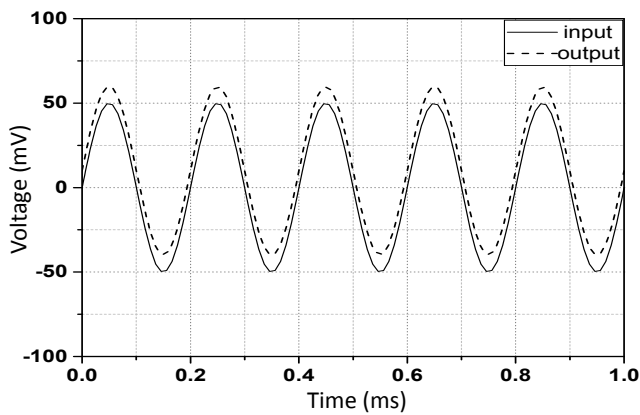

**Fig. 10:** Time domain waveform of low pass response.

chosen as 10 kΩ and 100 pF, respectively. The values of $k = 1$, 2 and 4 are taken to obtain gain of 1, 2 and 4, respectively. The simulated response is depicted in Fig. 12, which agrees with theoretical predictions.

The SPICE simulations are also performed to observe the time domain behavior. All resistances and capacitances are kept at 10 kΩ and 100 pF, respectively. A 5 kHz sinusoidal input of 50 mV amplitude is applied to the filter and the low pass transient response is depicted in Fig. 10. Total harmonic distortion is also measured by changing input sinusoid amplitude and its value was found to be within 3 % till 150 mV amplitude. Another simulation is done by applying three sinusoids having frequencies of 10 kHz, 100 kHz and 1 MHz, respectively. Figure 13 shows the input and output waveforms and corresponding frequency spectrums. It is clear that the sinusoid having 1 MHz frequency is significantly attenuated.

Monte Carlo simulations are also done to check robustness of the proposed circuits by considering Gaussian distribution for fifty runs with 5 % variations in all passive components. For brevity, the histogram of circuit from Fig. 8(a) at LPF node output is depicted

(a)
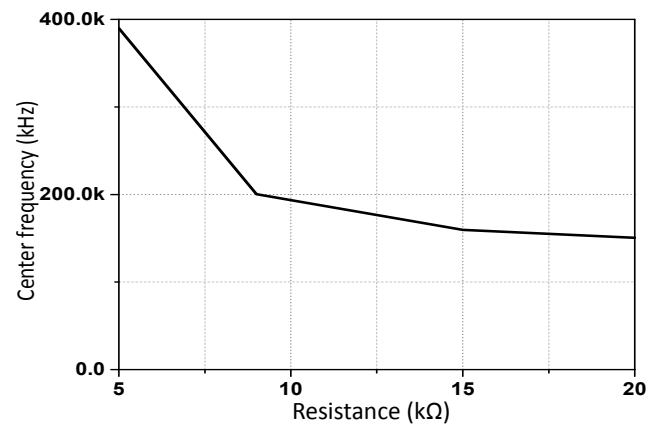
(b)
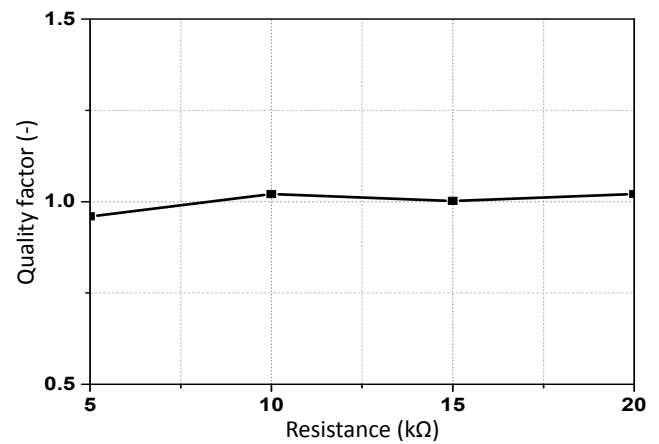
(c)

Fig. 11: Simulated (a) band pass frequency response, (b) center frequency and (c) Q variation.

in Fig. 14, it implies the circuit is well operated within the theoretical frequency.

The performance parameters related to power consumption, THD and output noise are presented in [11], [12], [13] and [14]. The same is placed in Tab. 1. The higher power consumption of the proposed topology in

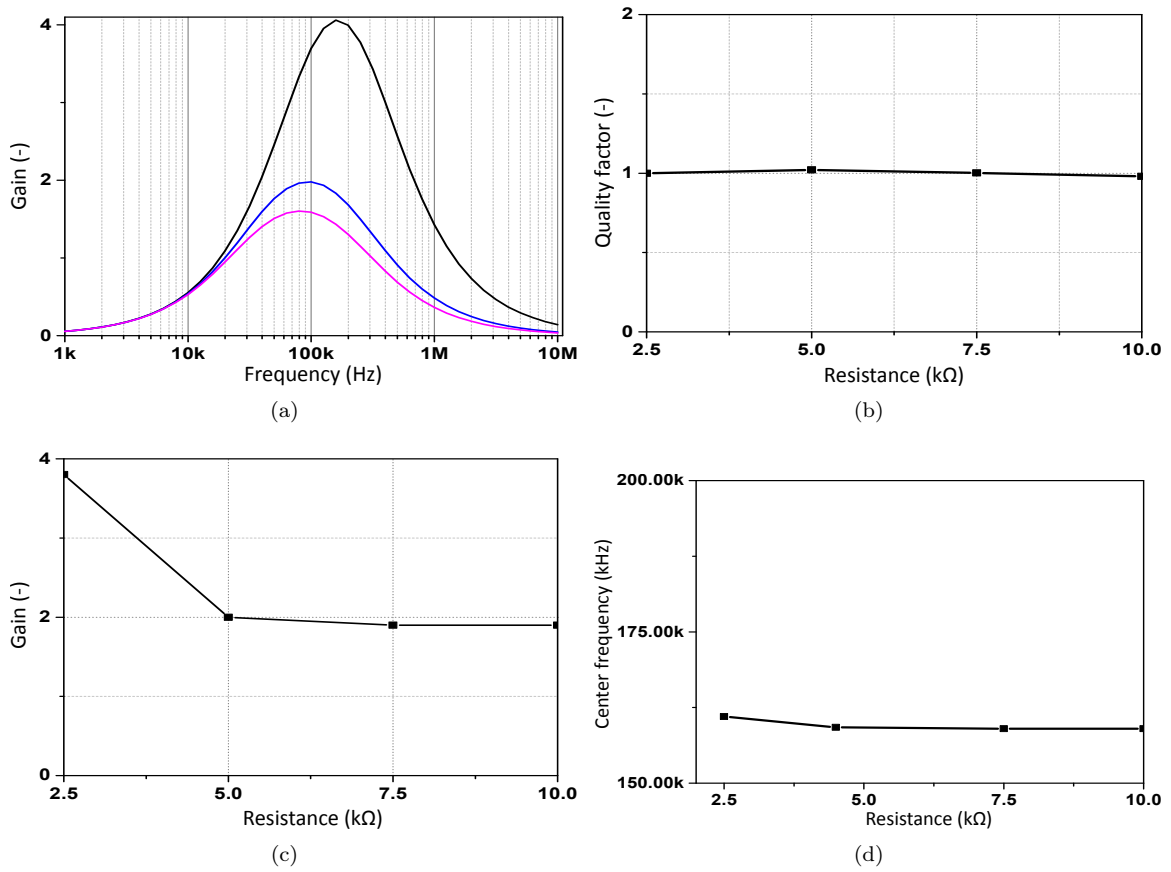**Fig. 12:** Simulated (a) frequency band pass response, (b) Q variation, (c) gain variation and (d) center frequency variation.
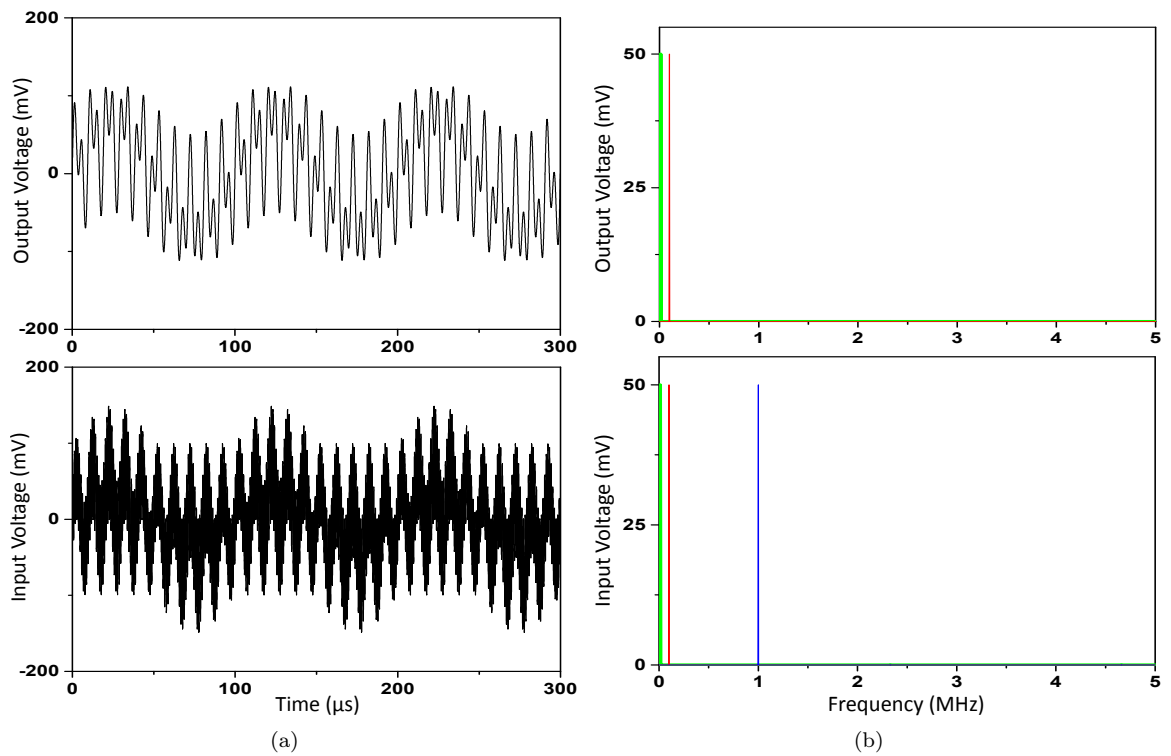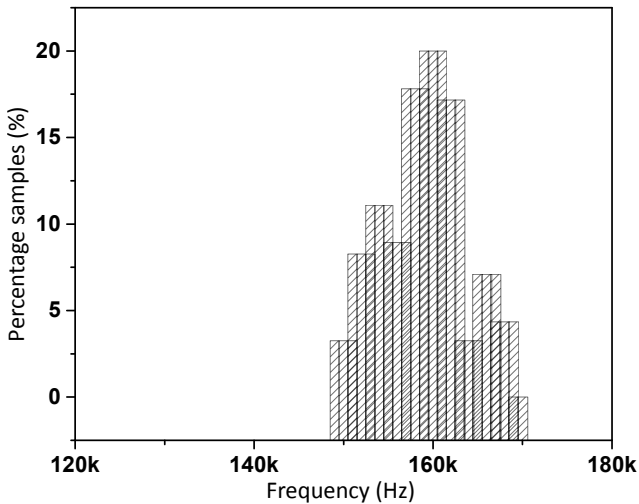

Fig. 13: Simulated transient low pass response (a) input and output waveforms and its (b) frequency spectrum.

Tab. 1: Summary of performance parameters.

Ref.	OTRA implementation	Power consumption (%)	THD (%)	Output noise ($\mathbf{\mu V \cdot Hz}^{-\frac{1}{2}}$)
[11]	CMOS based	4.04	1.7	–
[12]	CFOA based	421	–	4
[13]	CMOS based	2.58	5.7	0.722
[14]	CMOS based	1.09	6.74	0.316
Proposed	CMOS based	6	3	0.140

Fig. 14: Monte Carlo simulation results.

compatison with other CMOS-based OTRA implementations may be observed. However, the output noise for the proposed topology is lowest.

5.   Conclusion

An alternate realization for Single Input Multiple Output (SIMO) filter topologies has been presented in this contribution wherein differentiator is used as basic building block. An SFG is proposed for this purpose, which can further be used to derive sixteen SFGs through proper selection of inverting and non-inverting differentiators placed in loop; and their addition. The active block OTRA is used to verify the concept. All the realizations use three OTRAs, six resistors and two capacitors. The bandwidth and quality factor of these configurations can be adjusted independently of the pole frequency. The functional verification of the proposed method is done through SPICE simulations using 0.18 µm CMOS technology parameters from MOSIS.

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