A Novel Reduced Components Model Predictive Controlled Multilevel Inverter for Grid-Tied Applications

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Abstract. *This paper presents an improved single-phase Multilevel Inverter (MLI) which is conceptualized to reduce power switches along with separate DC voltage sources. Compared with recent modular topologies, the proposed MLI employs a reduced number of components. The proposed inverter consists of a combination of two circuits, i.e., the level generation and polarity generation parts. The level generation part is used to synthesize different output voltage levels, while the polarity inversion is performed by a conventional H-bridge circuit. The performance of the proposed topology has been studied using s single-phase seven-level inverter, which utilizes seven power switches and three independent DC voltage sources. Model Predictive Control (MPC) is applied to inject a sinusoidal current into the utility grid which exhibits low Total Harmonic Distortion (THD). Tests, including a change in grid current amplitude as well as operation under variation in Power Factor (PF), have been performed to validate the good performance obtained using MPC. The effectiveness of the proposed seven-level inverter has been verified theoretically using MATLAB Simulink. In addition, Real-Time (RT) validation using the dSPACE-CP1103 has been performed to confirm the system performance and system operation using digital platforms. Simulation and RT results show improved THD at 1.23 % of injected current.*

Keywords

Current control, grid-connected inverter, model predictive control, multilevel inverter, real-time.

1. Introduction

Voltage Source Inverter (VSI) can be considered as an industry standard for DC to AC conversion systems. The progress of power electronics leads to the requirement of VSI for many applications such as renewable energy systems, UPS, motor drives, [1], [2], [3] and [4]. Traditionally, the inverter is an H-bridge circuit which has the ability to develop a three-level output voltage waveform. However, the three-level output voltage has a bad harmonic profile [5]. For enhancing the quality of inverter output waveform, Multilevel Inverters (MLI), which provide staircase waveforms and improved harmonic profile, are a possible solution.

Conventional topologies of MLI are extensively studied and can be classified as; Neutral Point Clamped (NPCMLI), Flying Capacitor (FCMLI), and Cascaded H-bridge (CHBMLI) [6], [7] and [8]. CHBMLI has been considered as the best approach for increasing the number of levels due to modularization, low cost, and simplicity of implementation. However, increasing the number of levels with the CHBMLI leads to increased cost as well as reduced inverter efficiency. On the other hand, using a lower number of levels requires a large value of the LC output filter to reduce the harmonics content to an acceptable limit [9].

Most researchers are concerned with topologies that offer good harmonic profile and low cost. In [10], a single-phase seven-level transformer-less inverter was presented. However, it utilizes a high number of conducting devices for each output voltage level that leads to higher power loss. A five-level inverter was presented in [11] using four DC voltage sources, while the same number of DC voltage sources can generate a higher number of voltage levels in conventional topologies. A seven-level MLI was presented in [12] and modified

in [13] to develop a nine-level MLI. These topologies offer good multilevel performance. However, the non-modular structure of these topologies is the main restriction. In [14], MLI was generated thanks to the multi-winding transformer, but the cost is high for high power applications. In [15], a five-level inverter was proposed utilizing only six power switches with two isolated DC power supplies. However, it increases the system cost and size, in addition, non-modularity for increasing output voltage levels is not feasible. A five-level inverter was proposed in [16] by using six power switches and coupled inductors. However, the coupled inductors increase the overall cost, size, and weight. A four-level inverter was proposed in [17], however, this topology is valid only for even voltage levels and not able to provide zero states. In order to overcome the aforementioned problems, a new MLI is proposed to provide an output voltage with fewer numbers of components. The proposed inverter is investigated at seven-level output voltage with only seven power switches and three independent DC voltage sources.

The control strategies play a crucial role in the investigation of MLI for voltage or current control to ensure reliable and efficient operation [18]. For a grid-connected MLI, the output voltage is nearly constant in this case, the current is being controlled to control power transmitted to the grid. Grid-connected MLI plays an emerging topic in power systems. Therefore, the harmonic generated by the injected current must be limited to a low value to follow the IEEE harmonic factor standard [19]. As power quality is a significant point, the current controller must provide high quality with minimal harmonics. Several Current control topologies have been studied which concerning MLI like Proportional-Integral controller (PI), Hysteresis Current Control (HCC), Proportional-Resonance control (PR) [20], etc. All those controllers have some drawbacks; moreover, thanks to the advance in technology and DSP controllers that handle faster calculations, a Model Predictive Controller (MPC) becomes a powerful method for power converter applications. MPC receives great attention due to its facility in a wide range of power converters and drives applications [21].

The goal of this paper is to connect the proposed MLI to the grid with a good dynamic performance and low harmonic content. A seven-level inverter for grid connection is presented in this paper, where the injected current is controlled using MPC. This paper is organized as follows: the general structure for the proposed inverter and the generation of seven-level inverter with its possible states are presented in Sec. 2. and Sec. 3. respectively. Discrete-time model for the inverter using MPC and the current control scheme are provided in Sec. 4. and Sec. 5. respectively. Section 6. and Sec. 7. provide simulation results and real-time validation, respectively. Section 8. presents a comparative study with different topologies. Finally, Sec. 9. concludes the main results.

2. General Structure of the Proposed MLI

The proposed structure for MLI is shown in Fig. 1. It consists of two circuits; the Level Generation (LGP) and Polarity Generation Parts (PGP). The LGP contains a number DC voltage source (N_{DC}) which can be replaced with series-connected capacitors supplied from a single DC voltage source instead of using multiple DC voltage sources and power switches (N_{SW}) as is responsible for providing different voltage levels. The PGP is a traditional H-bridge circuit as it has two functions; controlling the polarity of different output voltage levels in addition to generating the zero-voltage states. As shown, the proposed inverter consists of n number of cells. Each cell is composed of one DC voltage source (or DC capacitor) in series with one power switch without body diode to avoid a short circuit between sources. Only the 1st cell has a power switch with an anti-parallel diode where, the function of the diode is to produce the first levels ($\pm V_{DC}$), while the power switch is to provide a free-wheeling path with inductive loads.

For series-connected capacitors, the voltage across capacitors will deviate during the switching process for the generation of output voltage levels. Therefore, the voltage balance across series-connected capacitors can be achieved by modifying the modulation technique [12] or using a voltage balancing circuit [12], etc. The relation between, N_{DC}, and N_{SW} based on the number of levels, N_{LEVEL} are calculated as follows:

$$N_{DC} = \frac{1}{2}(N_{LEVEL} - 1), \tag{1}$$

$$N_{SW} = \frac{1}{2}(N_{LEVEL} - 1) + 4. \tag{2}$$

The important parameter of MLI is Total Standing Voltage (TSV) also named by maximum blocking voltage of the inverter (Vb_{inv}). The selection of power switches is based mainly on the blocking voltage across it because this value determines the power rating of switches. As this value is reduced, the total cost of the inverter will also be reduced. The blocking voltage of power switches in LGP is equal to:

$$Vb_{s1} = Vb_{s2} = Vb_{s3} = ... = Vb_{sn} = V_{DC}. \tag{3}$$

While the blocking voltage of power switches in PGP (H-bridge circuit) is equal to the amplitude of the out-

Tab. 1: Switching states.

Voltage vectors		Output levels	Switching states						
			S1	S2	S3	Q1	Q2	Q3	Q4
+ ve	V_0	0	0	0	0	0	1	0	1*
	V_1	$3V_{DC}$	0	0	1	1	1	0	0
	V_2	$2V_{DC}$	0	1	0	1	1	0	0
	V_3	V_{DC}	1*	0	0	1	1	0	0
	V_4	0	0	0	0	1	0	1*	0
− ve	V_5	0	0	0	0	1*	0	1	0
	V_6	$-V_{DC}$	1*	0	0	0	0	1	1
	V_7	$-2V_{DC}$	0	1	0	0	0	1	1
	V_8	$-3V_{DC}$	0	0	1	0	0	1	1
	V_9	0	0	0	0	0	1*	0	1

1* denotes current flow through the body diode where 1=ON & 0=OFF.

put voltage based on the following equation:

$$Vb_{Q1} = Vb_{Q2} = Vb_{Q3} = Vb_{Q4} = V_{ab\,\max} = n \cdot V_{DC}. \tag{4}$$

Where, $V_{ab\,\max}$ is the maximum amplitude of the generated output voltage. TSV equals to total blocking voltage of power switches in LGP (Vb_{LGP}) and PGP (Vb_{PGP}) and can be calculated as presented in the following equations,

$$Vb_{LGP} = Vb_{s1} + Vb_{s2} + Vb_{s3} + ... + Vb_{sn} = nV_{DC}. \tag{5}$$

$$Vb_{PGP} = Vb_{Q1} + Vb_{Q2} + Vb_{s3} + Vb_{sn} = 4 \cdot nV_{DC}. \tag{6}$$

$$TSV = Vb_{inv} = 5 \cdot nV_{DC}. \tag{7}$$

From Eq. (7), the maximum blocking voltage based on number of cells and the value of DC voltage sources.

As seen from Eq. (4), this topology is not suitable for high voltage application as stress in H bridge carry total rated output voltage of the inverter. The proposed inverter can be used with application requires power ranges less than 10 kW. In order to be used with higher power, cascaded connection from the proposed topology can be used.

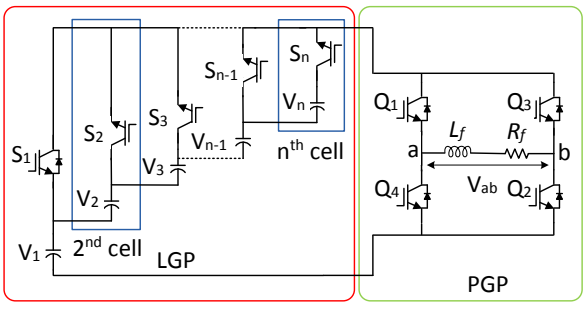
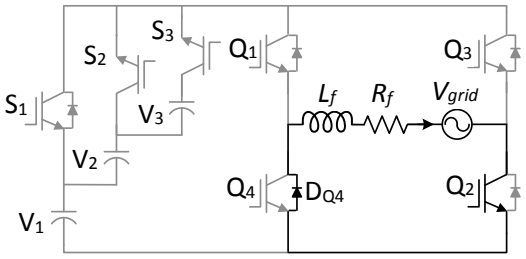


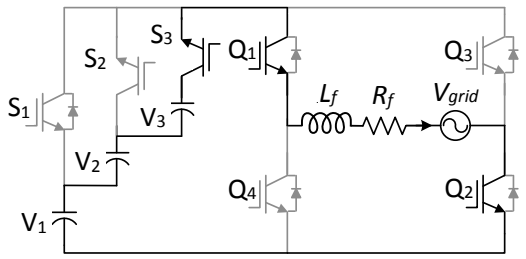
Fig. 1: Proposed multilevel inverter.

3. Seven-Level Output Voltage

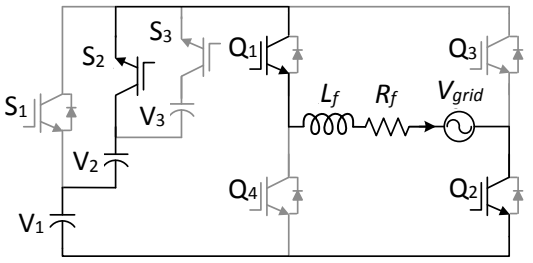
The construction of the proposed seven-level inverter is shown in Fig. 1. It consists of seven power switches and three cells with three DC voltage sources. It generates seven levels, i.e. 0, $\pm V_{DC}$, $\pm 2V_{DC}$, and $\pm 3V_{DC}$. The proposed topology has ten voltage vectors with four zero vectors, three in each positive and negative active vectors as depicted in Fig. 2. Table 1 presents possible states.



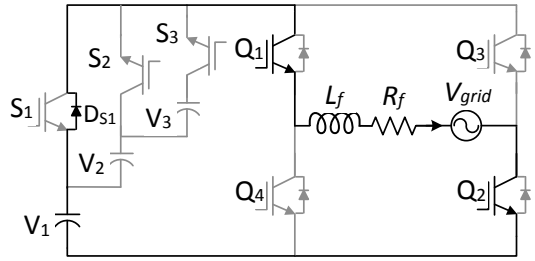
(a) V_0.



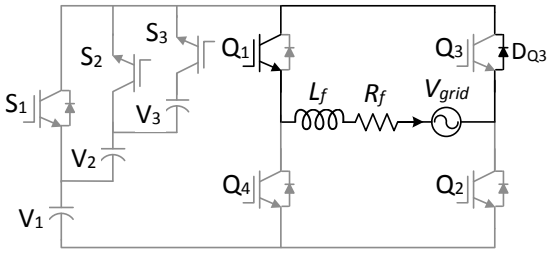
(b) V_1.



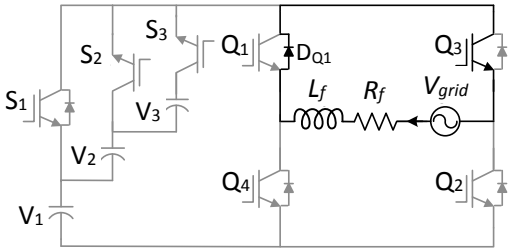
(c) V_2.



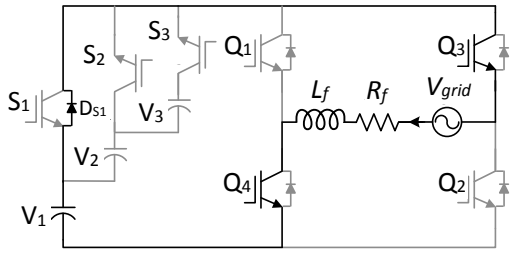
(d) V_3.



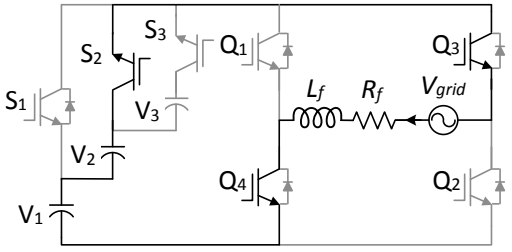
(e) V_4.



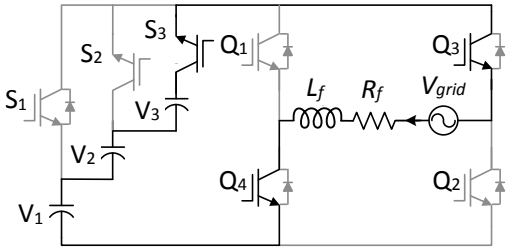
(f) V_5.



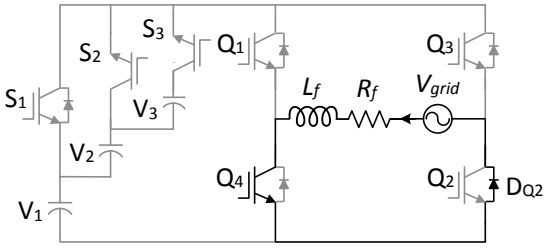
(g) V_6.



(h) V_7.



(i) V_8.



(j) V_9.

Fig. 2: Possible states of grid-connected seven-level inverter.

4. Model Predictive Control for the Proposed Seven-Level Inverter

MPC predicts the behavior of variables for a finite number of possible switching states. It can be applied in different applications, i.e. AC/DC, AC/AC, and DC/AC converters. The predictive control scheme for a grid-connected DC/AC converter is shown in Fig. 3. The flexibility of the controller makes it a better choice to control different variables. For grid-connected inverter, the control variable is the current injected to the grid. The control strategy can be summarized as follow:

- Describe the continuous-time model of the system.
- Finding discrete-time model of the system based on sampling time.
- Present the voltage vectors which describe the voltage levels for the presented inverter.
- Measuring injected current to the grid at the instant sample time.
- Use discrete model along with the measured value of the injected current to predict the behaviour of the controlled variable, i.e. the injected current at the next sampling time for all possible voltage vectors generated by the converter.
- Calculating the cost function for each prediction.

- The voltage vector that minimized the cost function is selected, and its corresponding switching combination is applied to the power converter.

The injected current is measured at sampling time (K), and the optimal switching states are instantly presented. The switching state which presents minimum cost function is calculated at sampling time $(K+1)$ and applied at sampling time (K).

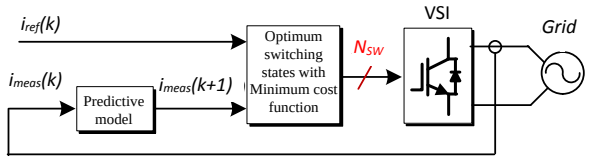


Fig. 3: Model predictive control scheme in DC/AC converter.

To control the seven-level inverter's injected current (i_{meas}), a discrete-time model for the current control must be defined. According to the equivalent circuit shown in Fig. 4, the continuous-time expression for i_{meas} can be expressed as follows:

$$V_o = V_{grid} + R_f i_{meas}(t) + L_f \frac{\mathrm{d}i_{meas}(t)}{\mathrm{d}t}, \qquad (8)$$

where, V_o and V_{grid} are the inverter's output voltage and grid voltage, respectively. R_f and L_f are the grid filter resistance and inductance, respectively. By rearranging Eq. (8):

$$\frac{\mathrm{d}i_{meas}(t)}{\mathrm{d}t} = \frac{V_o - V_{grid} - R_f i_{meas}(t)}{L_f}. \qquad (9)$$

According to Euler's method, with a sample time T_s, the derivative term in Eq. (9) can be expressed as follows:

$$\frac{\mathrm{d}i_{meas}(t)}{\mathrm{d}t} = \frac{i_{meas}(k+1) - i_{meas}(k)}{T_s}. \qquad (10)$$

Therefore, the discrete-time model for i_{meas} can be expressed as follows:

$$i_{meas}(k+1) = \frac{T_s}{L_f}(V_o - V_{grid}) + (1 - \frac{T_s R_f}{L_f}) i_{meas}(k). \qquad (11)$$

Equation (11) is used to predict the behaviour of the injected current at the next sampling interval for all voltage vectors. The required control function here is controlling the amplitude and frequency of the injected grid current according to the reference value (i_{ref}), therefore the cost function (g) will be:

$$g = \mid i_{ref}(k) - i_{meas}(k+1) \mid . \qquad (12)$$

Figure 5 depicts the flow chart of the MPC algorithm. As can be seen, the switching states of the power switches are generated according to the minimum cost function.

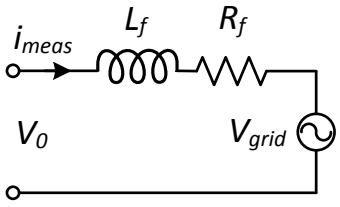


Fig. 4: The equivalent circuit of the multilevel inverter.

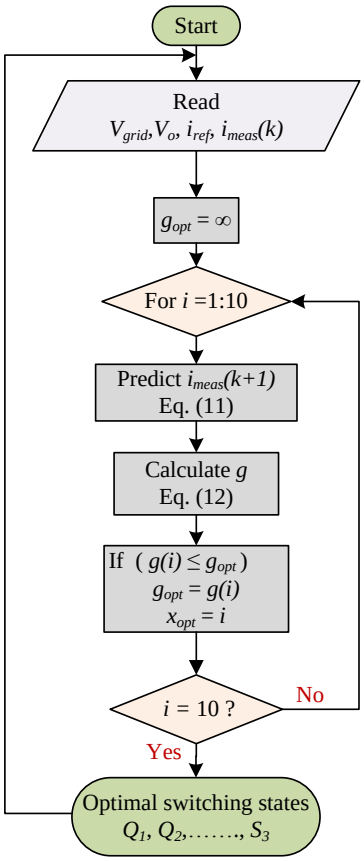


Fig. 5: Model predictive control algorithm.

5. Current Control Strategy

Figure 6 shows the current control scheme, which comprises grid-connected seven-level inverter under the MPC technique. R_f and L_f are applied to tie the inverter to the grid. The closed-loop control is applied to control the value of i_{meas}. Phase-Locked Loop (PLL) is used to generate i_{ref} according to the grid voltage. To ensure the effectiveness of the control has been used, a step change in the amplitude of i_{ref} to provide different amounts in the injected power to the

grid. Furthermore, a phase shift is applied to the angle generated from PLL in order to change the Power Factor (PF).

i_{meas}, V_o, and V_{grid} are the inputs to the predictive model, according to Eq. (6) and the output will be the predictive value of i_{meas} at the next sample time. i_{ref} at the instant sample time and i_{meas} from Eq. (6) are used to calculate g. With the minimum value of g, the corresponding switching states for the seven switches are applied to the power switches.

6. Simulation Results

Simulation of the proposed seven-level inverter controlled by MPC under grid connection for current control has been validated using MATLAB Simulink. For analysis, the voltage across the three series-connected capacitors are assumed constant over the switching cycle and replaced by three independent DC voltage sources.

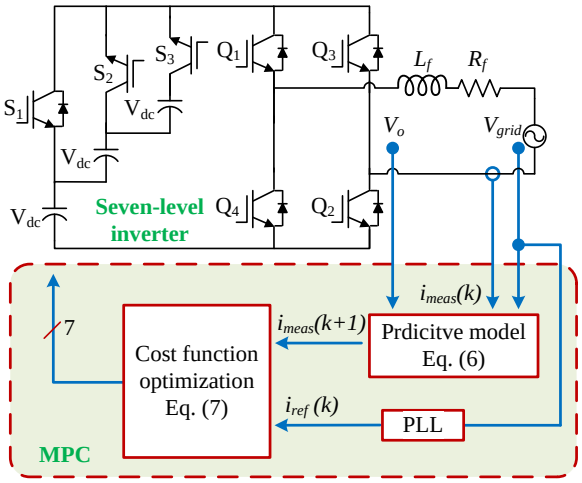


Fig. 6: Current control scheme for the proposed single-phase seven-level inverter.

In the simulation, V_{grid} is set to 220 V RMS with fixed a frequency, i.e. 50 Hz. Three cells with seven-level inverter have three DC sources ($V_1 = V_2 = V_3$) with a peak value of 110 V. The value of DC voltage sources are taken to be greater than $\sqrt{2}$ value of V_{grid} to ensure power transfer to the grid. Grid parameters are $R_f = 0.5\ \Omega$ and $L_f = 1$ mH. The results have been obtained with $T_s = 2\ \mu$s.

Figure 7 presents the simulation results of a grid-tied seven-level inverter. Figure 7(a) shows the inverter output voltage and grid voltage. It can be observed that the proposed inverter synthesizes seven-level output voltage including 0 V, ±110 V, ±220 V and ±330 V. While Fig. 7(b) presents the actual grid current and grid voltage. As seen, the actual grid current is in phase with the grid voltage which ensures that unity PF is effectively achieved.

A Step change in the amplitude of reference grid current is provided to certify the performance of the proposed inverter under different amount of injected power, as shown in Fig. 8. Furthermore, Fig. 8(a) provides the injected grid and reference currents. Figure 8(b) shows the step response of the injected grid current to track its reference current. It can be observed that the injected current effectively tracks its reference value where its dynamic response is fast. Consequently, at first, the active power is 624.3 W, and after a step change, the active power is 831.6 W.

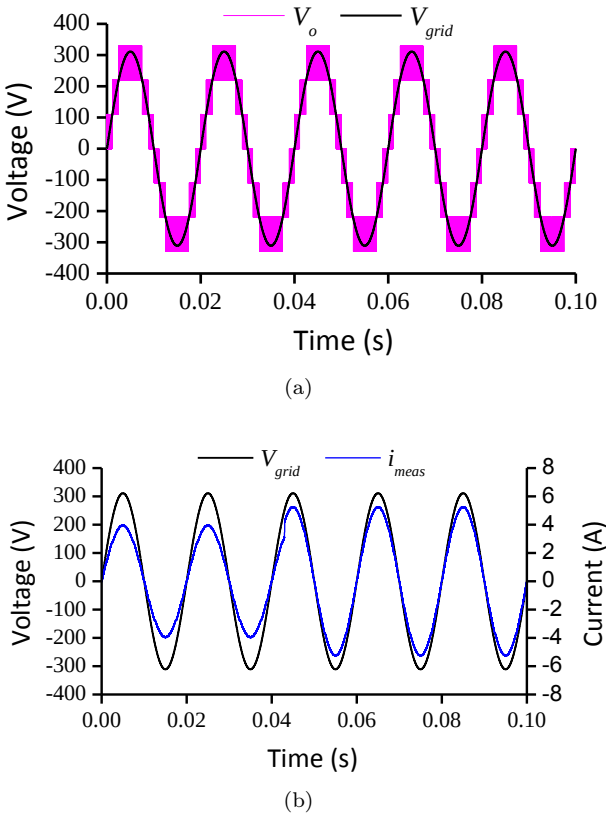


Fig. 7: Voltage and current waveforms for a grid-connected inverter with unity PF.

Besides the capability of tracking the reference value, another important performance measure is the harmonic spectrum for the injected current to the grid by using Fast Fourier Transform (FFT). Fig. 9 presents FFT analysis for the injected grid current. As seen, it provides low harmonic content, which significantly leads to low switching losses and less filter. Also, a major concern for a grid-connected MLI is the Total Harmonic Distortion (THD) of the injected current. It can

be calculated as follows:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} i_n^2}}{i_1}. \quad (13)$$

It must meet the host grid requirements of value less than the IEEE standard of 5 %. The analysis of THD in the injected current is found to be 1.23 % up to 250 kHz.

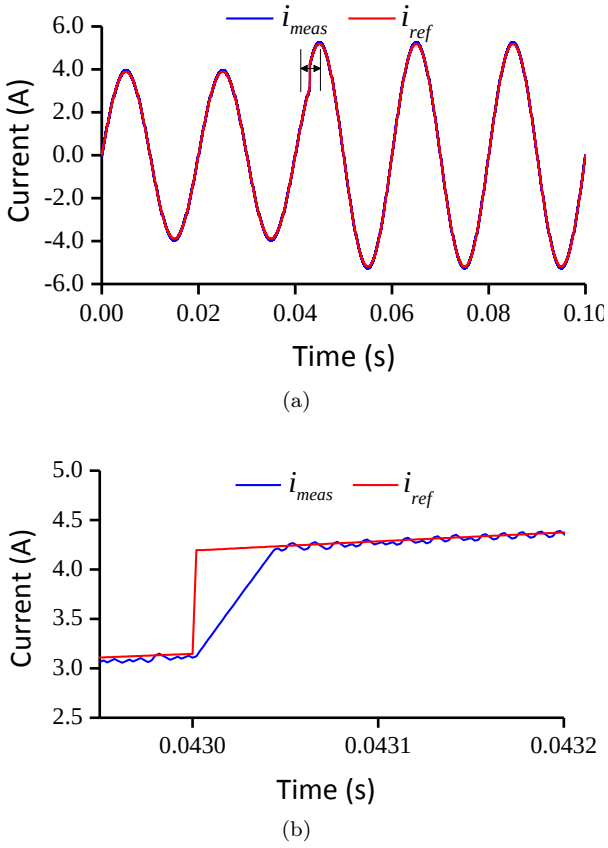


Fig. 8: The injected grid and reference currents waveforms under a variation on the amplitude of reference current.

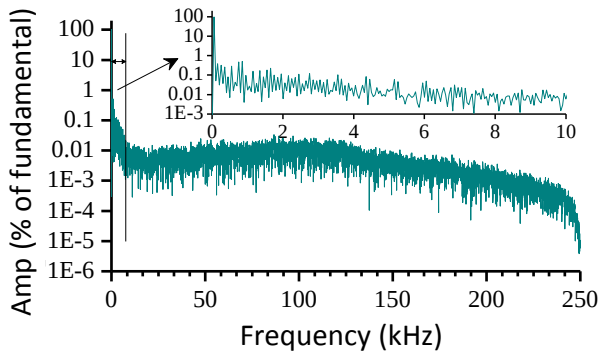


Fig. 9: FFT analysis of the injected current.

In Fig. 10, another change has been implemented aiming to exchange reactive power with the grid.

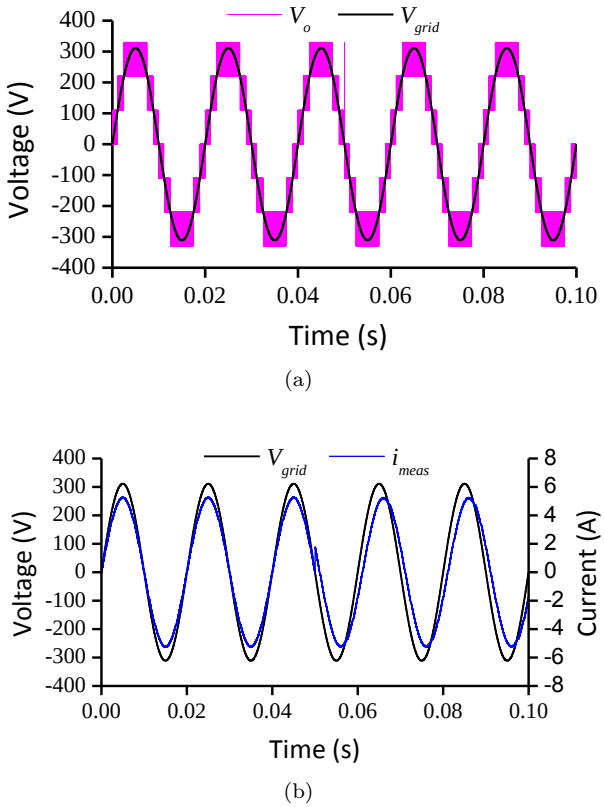
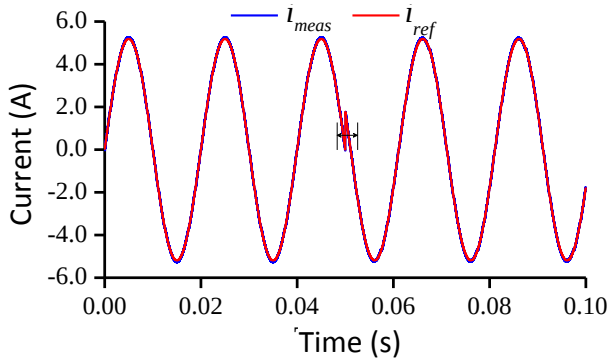


Fig. 10: Voltage and current waveforms for a grid-connected inverter with 0.94 PF.

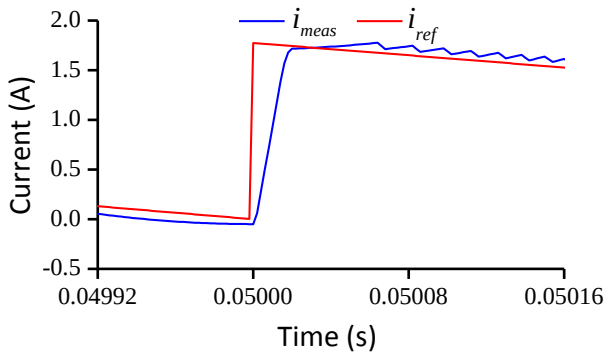
A sudden change has been made in the phase shift from 0° to 20° in the angle between the grid voltage and injected current to ensure a change of PF from unity to 0.94. Accordingly, the active power is 781.04 W while the reactive power is 284.12 VAR. Figure 10(a) presents the inverter output voltage and grid voltage. One can be noticed that the inverter output voltage is not affected by the change in PF. Figure 10(b) presents the actual grid current and grid voltage. As it is clear, both grid current and grid voltage are in phase which presents unity PF and then have a change with 20° phase shift. Eventually, in order to confirm the dynamic performance of the MPC, Fig. 11(a) and Fig. 11(b) provides the injected grid and reference currents. As seen the injected current follows reference value at fast response.

7. Real-Time Validation

The performance of the proposed inverter for grid-tied application with a Real-Time (RT) setup has been performed and compared with simulation results. RT simulation is performed using MATLAB/SIMULINK and dSAPCE-CP1103 control desk, as shown in Fig. 12.



(a)



(b)

Fig. 11: The injected grid and reference currents waveforms under a variation on the phase shift of reference current.

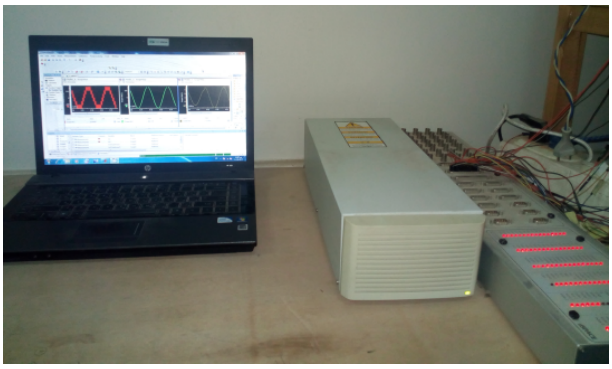
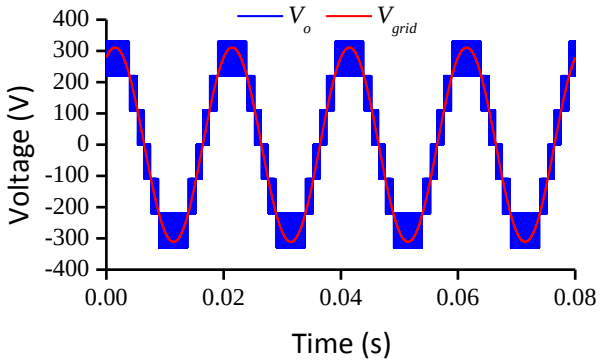
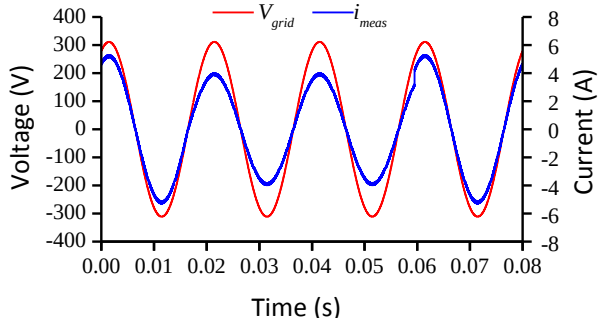


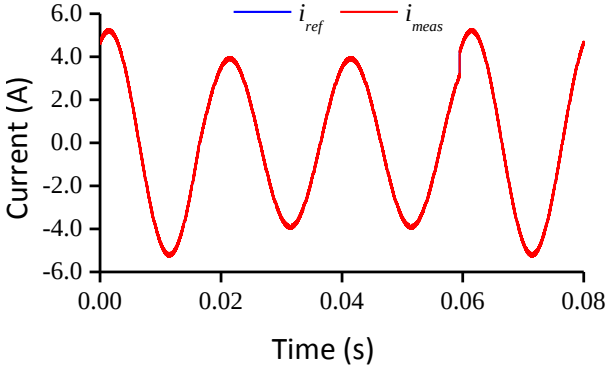
Fig. 12: Photograph for RT system.



(a)



(b)



(c)

Fig. 13: Real-time results of seven-level grid-connected inverter.

The RT results are illustrated in Fig. 13 with a fixed sampling time of 2 μs as used in the simulation.

The inverter output voltage and the grid voltage are displayed in Fig. 13(a). As can be seen, the inverter terminal voltage has seven levels, which match the simulation results. To ensure unity PF, Fig. 13(b) presents the grid voltage and injected current. The grid voltage and the injected current, as shown, are well synchronized, and unity PF mode has been achieved successfully. The measured and reference grid current is displayed in Fig. 13(c). As can be observed, the reference value is tracked effectively by the measured current, which provides good performance as observed by simulation results.

8. Comparative Study of the Proposed Inverter with Existing Topologies

To present the effectiveness of the proposed topology over other recent topologies, comparisons must be

Tab. 2: Comparative analysis to obtain symmetrical single-phase seven-level inverter.

MLI type	Components						
	N_{DC}	N_{SW}	N_C	N_D	N_T	$LSratio$	TSV
[11]	1	12	6	12	31	0.583	20 V_{DC}
[12]	3	7	0	2	12	1.000	19 V_{DC}
[23]	3	12	0	0	15	0. 583	12 V_{DC}
[24]	3	10	0	0	13	0.700	18 V_{DC}
[25]	3	9	0	0	12	0.778	17 V_{DC}
[26]	3	8	0	0	11	0.875	12 V_{DC}
[27]	3	8	0	0	11	0.875	16 V_{DC}
Proposed	**3**	**7**	**0**	**0**	**10**	**1.000**	**15 V_{DC}**

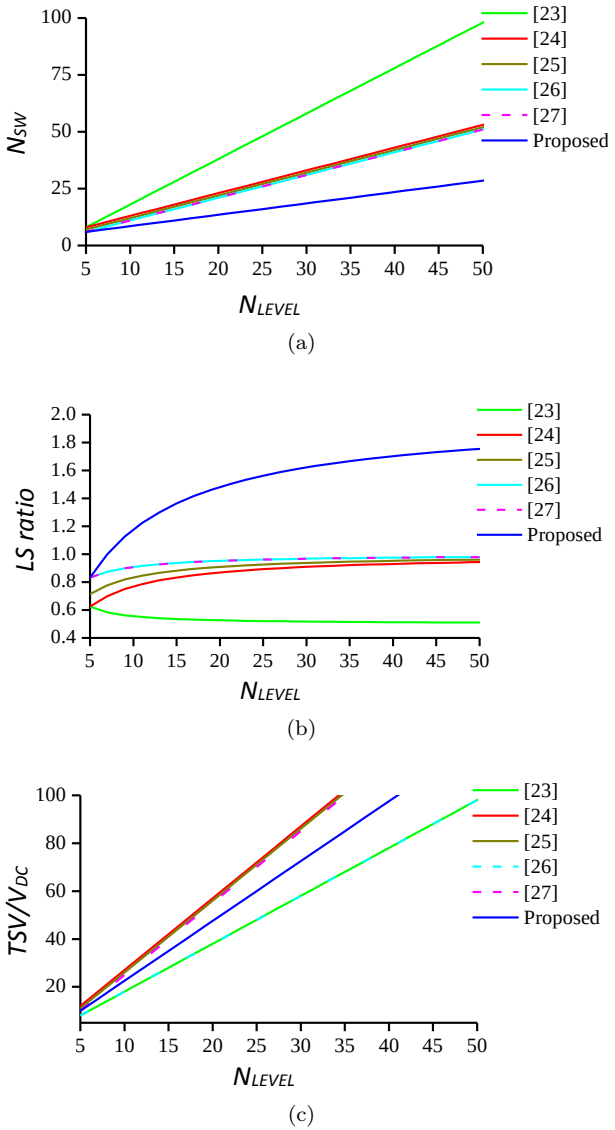


Fig. 14: Comparison between different topologies and proposed inverter.

made. The main aim of presenting any topology is the increasing the number of output voltage levels while using as lower number of components as possible, in addition, total standing voltage of the presented topology. Therefore, several comparisons have been made in this section. First, Tab. 2 presents a comparison between different topologies with the proposed topology for symmetrical seven-level output, which can be obtained from its structure. The comparison is made under the following parameters; N_{DC}, N_{SW}, number of clamping capacitors (N_C), number of diodes (N_D), and total number of components (N_T). In addition, the parameter number of level to power switch ratio (LS ratio) is also calculated. As shown from Tab. 2, the proposed inverter provides less number of components compared with other topologies for the same number of levels.

In modular topologies, MLI can generate higher levels with the same subunits. In the proposed topologies, subunit contains a cell which has one DC voltage source along with one power switch. Therefore, Fig. 14 presents comparisons with modular topologies based on N_{LEVEL}. Fig. 14(a) shows a comparison between N_{SW} and N_{LEVEL} for different topologies. As shown, the proposed inverter provides less number of N_{SW} compared with other topologies for the same number of levels. Fig. 14(b) presents the LS ratio versus N_{LEVEL}. As presented, the proposed topology provides the higher value of LS ratio, which presents fewer power switches for higher levels, in addition, fewer conduction losses compared with other topologies. Finally, Fig. 14(c) provides TSV with the change in the number of levels. As is obvious, the TSV in the proposed inverter is higher than some MLI such as presented in [23] and [26]. Therefore, it limits the application of the proposed inverter for high voltage applications, but it still has merits in comparison with the presented topologies of higher LS ratio in addition, lower N_{SW}.

9. Conclusion

This paper presented a new single-phase DC/AC multilevel inverter with a low number of components for the grid-tied application. Seven-level inverter was presented, which has seven power switches with three identical DC power supplies. The injected current to the grid was controlled using model predictive control. In this paper, the seven-level inverter tied to the grid with THD at 1.23 %. The results showed a fast response in

controlling the injected current during a step change in the injected grid current in its amplitude rather than its phase shift from the grid voltage. The inverter had been validated using computer software and verified using real-time by dSPACE-1103. It was cleared that the real-time results match the simulation results.

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