

# A NOVEL REALIZATION OF LOW-POWER AND LOW-DISTORTION MULTIPLIER CIRCUIT WITH IMPROVED DYNAMIC RANGE

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**Abstract.** A novel topology of four-quadrant analog multiplier circuit is presented in this paper. The voltage mode technique is employed to design the circuit in CMOS technology. The dynamic input and output ranges of the circuit are improved owing to the fact that the circuit works in the saturation region not in weak inversion. Also the proposed multiplier is suitable for low voltage operation and its power consumption is relatively low. In order to verify the performance of the proposed circuit, performance of the circuit affected by second order effects including transistor mismatch and mobility reduction is analyzed in detail. It will be shown that any conceivable mismatch in the transistor parameters leads to second harmonic distortion. Additionally, the effect of mobility reduction in the third harmonic distortion will be computed. In order to simulate the circuit, Cadence and HSPICE software are used with TSMC level 49 (BSIM3v3) parameters for 0.18  $\mu\text{m}$  CMOS technology, where under supply voltage of 1.5 V, total power consumption is 44  $\mu\text{W}$ , the corresponding average nonlinearity remains as low as 1 %, and the input range of the circuit is  $\pm 400$  mV.

## Keywords

CMOS design, four quadrant, low distortion, modulation, multiplier circuit.

## 1. Introduction

In recent years, analog multipliers are widely used in many applications such as phase-locked loops, adaptive

filters, modulators, automatic gain controlling, image processing, artificial neural networks and fuzzy integrated systems [1], [2], [3] and [4]. Different methods of implementation of this building block have been recently presented based on the use of bulk driven MOS [5], Floating Gate MOS (FGMOS) [6] and class-AB mode [7]. In the past decade, the demand for portable operation of electronic systems has led to the trend of designing circuits to be featured with low power consumption and operate for low supply voltages. One possible technique to design the low-power dissipation multiplier circuit is to use MOSFETs in sub-threshold region [8], [9] and [10] in which most of them follow the Gilbert cell topology and modified Gilbert cell [11]. The drawback of designs in this region has been referred to poor dynamic range, limited bandwidth and low voltage swing. Another approach of designing low power multiplier circuits is to use the translinear principle of MOS transistors operated in the weak inversion [12] and [13]. Although this approach has the advantage of low power consumption, the dynamic range of these circuits is very small and operation speed is slow. On the contrary, presented multipliers based on the translinear loop in saturation region exhibit wider bandwidth, higher dynamic range and lower distortion and thus they are more preferred than those operating in weak inversion [14]. Nonetheless, the channel length modulation and body effect are the important issues in the circuits based on translinear loop principle. Another salient feature of the circuits is the four-quadrant operation capability, an important asset very useful in various applications [15] and [16]. Some of the well-known multiplier circuits operate only in one [17] and [18] or two quadrants [19] and [20], which was discussed in [21] and not suitable for many of mentioned applications.

Another factor, which is important in the multiplier circuit, is non-linearity factor, because of the fact that the multiplication operator is a linear map between input and output. Therefore this factor is a serious challenge in the multiplier circuits, which is commonly affected by body effect, mobility reduction and mismatch in the circuit devices. In some existing analog multipliers, the effects of these non-idealities were properly studied and a few techniques were proposed in order to reduce the non-linearity [22] and [23]. However, they suffer from low accuracy and/or low bandwidth. Moreover, single supply voltage circuits are preferred to those in dual mode [24], where the multipliers reported in [8] and [20] require dual supply voltage. As such these circuits are not suitable for today's world of portable equipment.

In this paper, a novel design of four quadrant analog multiplier is presented which benefits from advantages of differential output topology. The dynamic input and output ranges of the circuit are significantly improved. High linearity and high accuracy are further advantages of the circuit. Also the proposed multiplier is suitable for low voltage operation and its power consumption is relatively low. The performance of the proposed multiplier is characterized using HSPICE with TSMC in 0.18  $\mu\text{m}$  CMOS technology. The paper is organized in 5 sections: The proposed circuit is presented in Sec. 2, followed by the performance analysis in Sec. 3. In Sec. 4, HSPICE simulation results of proposed multiplier circuit are presented to prove the efficiency of the design. Finally, Sec. 5 concludes the most important achievement of the proposed circuit.

## 2. The Proposed Multiplier

The proposed four-quadrant multiplier circuit is shown in Fig. 1, which is based on the square-difference algebraic identity as:

$$(x + y)^2 - (x - y)^2 = 4xy. \tag{1}$$

According to this, to realize this equation, two squaring functions should be designed in which their outputs need to be subtracted. Let us consider the proposed circuit of Fig. 1. Assume that all of the transistors operate in saturation region (except for  $M_{17}$  and  $M_{18}$ ), thus the drain current of transistors by neglecting the second order effect such as mobility reduction and channel-length modulation can be expressed as:

$$I_D = K(V_{GS} - V_T)^2, \tag{2}$$

where  $K = 0.5\mu_0 C_{OX}(W/L)$  is related to transconductance parameter,  $V_{GS}$  is gate-to-source voltage and  $V_T$  represents the threshold voltage of MOS transistor which can be affected by body effect. The body effect refers to change in the transistor threshold voltage resulting from a voltage difference between the transistor source and substrate, which can be characterized by:

$$V_T = V_{t0} + \gamma \left[ \sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|} \right], \tag{3}$$

where  $V_{t0}$  is the zero-bias threshold voltage,  $\gamma$  is the body-effect coefficient and  $\phi_F$  is the Fermi potential. Considering the figure, two squaring circuits are shown in left half and right half of the structure. Focusing on the left side squaring circuit, since transistors  $M_1$  and  $M_2$  are biased in the saturation region and also  $I_{D1} = I_{D2}$ , the relationship can be written as:

$$K_N(V_{in} - V_1 - V_{TN})^2 = K_N(V_1 - V_{TN})^2. \tag{4}$$

Simplifying equation above we have:

$$V_1 = \frac{2V_{in}V_{TN} - V_{in}^2}{(-2V_{in} + 4V_{TN})} = \frac{V_{in}}{2}. \tag{5}$$

One can find the voltage of  $V_2$  at the same way as:

$$V_2 = -\frac{V_{in}}{2}. \tag{6}$$

The voltages of  $V_1$  and  $V_2$  are utilized to turn on  $M_9$  and  $M_{10}$  transistors, respectively. In this case, their

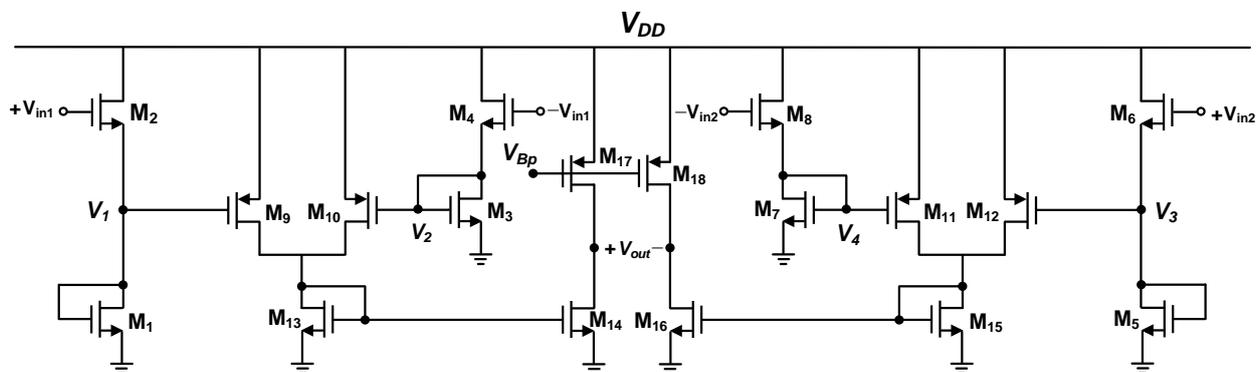


Fig. 1: The proposed four-quadrant analog multiplier circuit.

currents are added together and flow to transistor  $M_{13}$ :

$$I_{D13} = I_{D9} + I_{D10} = K_P [(V_{DD} - V_1 - |V_{TP}|)^2 + (V_{DD} - V_2 - |V_{TP}|)^2]. \quad (7)$$

Replacing Eq. (5) and Eq. (6) in Eq. (7); after few mathematical manipulations we have:

$$I_{D13} = 2K_P \left[ \left( \frac{V_{in1}}{2} \right)^2 + (V_{DD} - |V_{TP}|)^2 \right]. \quad (8)$$

It can be clearly seen from Eq. (8) that the current  $I_{D13}$  is the square of the input voltage plus some constant voltages. The same procedure can be followed for the right half of the circuit to obtain  $I_{D15}$ :

$$I_{D15} = 2K_P \left[ \left( \frac{V_{in2}}{2} \right)^2 + (V_{DD} - |V_{TP}|)^2 \right]. \quad (9)$$

The currents of  $I_{D13}$  and  $I_{D15}$  are transferred to the output through transistors  $M_{14}$  and  $M_{16}$ , respectively. Transistors  $M_{17}$  and  $M_{18}$  are biased in the triode region (by setting  $V_{Bp} = -1$ ) and perform as the resistors in which their resistance values can be represented by:

$$R_n \approx [\mu_n C_{ox}(W/L)_n(V_{SGn} - |V_{TP}|)]^{-1}. \quad (10)$$

By setting  $R_{17} = R_{18} = R$ , the output voltage of proposed circuit can be derived as:

$$V_{out} = R(I_{D14} - I_{D16}) = 2RK_P \left[ \left( \frac{V_{in1}}{2} \right)^2 - \left( \frac{V_{in2}}{2} \right)^2 \right]. \quad (11)$$

According to Eq. (11), by establishing  $V_{in1} = V_x + V_y$  and  $V_{in2} = V_x - V_y$  the ultimate voltage is eventually what would be expected as follows:

$$V_{out} = 2RK_P(V_x V_y). \quad (12)$$

Take notice that summation of the signals is provided by series connection of the voltage sources ( $V_x$  and  $V_y$ ). Also subtraction of the input signals was realized in the same way except for changing the polarity of  $V_y$ , which were performed using a well-known inverting amplifier. Also, there is no need subtraction at the output node, because the output is differential.

### 3. Performance Analysis

In this section, performance of the circuit affected by second order effects including transistor mismatch and mobility reduction is analyzed in detail. It will be shown that any conceivable mismatch in the transistor parameters leads to second Harmonic Distortion

(HD). Additionally, the effect of mobility reduction in the third harmonic distortion will be computed. Following that, the effect of corresponding parameters derived in each section as well as improvement methodology will be thoroughly discussed.

#### 3.1. Second HD Due to the Mismatch

In Sec. 2, the well-matched parameters including trans-conductance and threshold voltage of the transistors were assumed to obtain the output of the circuit. Considering Eq. (5), due to the fact that the voltage of  $V_1$  is resulted by supposing these matched parameters, any possible mismatch in the proposed circuit will affect the voltage of this node. Similarly, the voltages of  $V_2$ ,  $V_3$  and  $V_4$  get affected by the mismatch accordingly. Since these voltages have direct proportion to  $V_{in1}$  and  $V_{in2}$ , consequently the total mismatch is referred to the input signals and can be modeled as:

$$V_1 = \frac{V_{in1}}{2} + \Delta v_{in1} V_{in1}, \quad (13)$$

$$V_2 = -\frac{V_{in1}}{2} - \Delta v_{in1} V_{in1}, \quad (14)$$

$$V_3 = \frac{V_{in2}}{2} + \Delta v_{in2} V_{in2}, \quad (15)$$

$$V_4 = -\frac{V_{in2}}{2} - \Delta v_{in2} V_{in2}, \quad (16)$$

where  $\Delta v_{in1}$  and  $\Delta v_{in2}$  are mismatch percentages of  $V_{in1}$  and  $V_{in2}$ , respectively. By applying  $V_{in1} = V_x + V_y$  and  $V_{in2} = V_x - V_y$  to the multiplier circuit, the output voltage is given by:

$$V_{out} = 2RK_P [V_x V_y + (2\Delta v_{in1}^2)(V_x + V_y)^2 \dots \dots - (2\Delta v_{in2}^2)(V_x V_y)^2]. \quad (17)$$

It can be clearly seen that the terms of  $\Delta v_{in1}^2$  and  $\Delta v_{in2}^2$  are very small (because  $\Delta v_{in1}$  and  $\Delta v_{in2} < 1$ ), therefore the resulted error will be negligible. It is worthwhile to calculate the harmonic distortion of the circuit at the output considering the method presented in [25], if one of the inputs ( $V_x$ ) is kept constant and the other one is sinusoidal in the form of  $V_y = \hat{v}_m \sin t$ , second harmonic distortion can be derived as follows:

$$HD_2 = \frac{\Delta v_{in1}^2 - \Delta v_{in2}^2}{2V_x (4\Delta v_{in1}^2 + 4\Delta v_{in2}^2 + 1)} \hat{v}_m. \quad (18)$$

The equation implies that when the mismatch percentage of  $\Delta v_{in1}^2$  and  $\Delta v_{in2}^2$  increases, second harmonic distortion decreases. Also, it decreases with decreasing  $V_x$  as well.

### 3.2. Effect of Mobility Reduction in Third HD

If the mobility reduction is taken into calculations, the drain current of a MOS transistor operated in saturation is given by [26]:

$$I_D = \frac{K(V_{GS} - V_T)^2}{1 + \theta(V_{GS} - V_T)}, \quad (19)$$

where  $\theta$  is the mobility degradation parameter which varies typically from 0.001 to 0.1  $V^{-1}$ . This equation may be expanded in a Taylor series:

$$I_D = K(V_{GS} - V_T)^2 \cdot [1 - \theta(V_{GS} - V_T) + \theta^2(V_{GS} - V_T)^2 + \dots]. \quad (20)$$

To simplify the calculations, just the first order of  $\theta$  is used, and the higher-order terms are ignored. Replacing the expansion in Eq. (4), one can reach  $V_1$  and  $V_2$  as:

$$V_1 \approx \frac{V_{in1}}{2} + \frac{\theta V_{in1}(V_{in1}^2 - 3V_{in1}V_{TP} + 3V_{TP}^2)}{4V_{TP}}, \quad (21)$$

$$V_2 \approx -\frac{V_{in1}}{2} + \frac{\theta V_{in1}(V_{in1}^2 + 3V_{in1}V_{TP} + 3V_{TP}^2)}{4V_{TP}}. \quad (22)$$

The same procedure can be followed to obtain  $V_3$  and  $V_4$ . In this case, the output of the multiplier circuit can be represented as follows:

$$V_{out} \approx RK_P \left( V_{in1}^2 - V_{in2}^2 + \dots \dots \frac{\theta V_{DD}(2V_{in2}^3 - 2V_{in1}^3 - 3V_{in2}^2V_{TP} + 3V_{in1}V_{TP})}{V_{TP}} \right). \quad (23)$$

By applying  $V_{in1} = V_x + V_y$  and  $V_{in2} = V_x - V_y$ , the final output will be obtained. Since the output voltage includes third-order of the inputs, third harmonic distortion is achieved by keeping one of the inputs ( $V_x$ ) as a constant and the other one as sinusoidal. Again using the method presented in [25] we have:

$$HD_3 = \frac{\theta V_{DD}}{2V_x V_{TP} - 4\theta(3V_{TP} - V_x^2 + 2V_x V_{TP})} \hat{v}_m^2. \quad (24)$$

### 4. Post Layout Simulation Results

In this section, simulation results are presented using HSPICE with TSMC level 49 (BSIM3v3) parameters for 0.18  $\mu m$  CMOS technology so as to verify the performance of the proposed circuit. The simulation results are carried out after extracting the layout, which is drawn by Cadence software using single

poly and two metals (Metal1 and Metal2). Figure 2 shows the full layout of the circuit, in which the area is  $66.35 \mu m \times 58.2 \mu m$ . The aspect ratio of transistors is given in Tab. 1 and the supply voltage is 1.5 V. Considering the condition of triode region for PMOS transistors of  $M_{17}$  and  $M_{18}$ , choosing  $V_{Bp} = -1$  V guarantees that these transistors operate in the triode region and work as the active resistances. DC transfer characteristic of the circuit over a considerable range of the inputs is shown in Fig. 3, in which one of the inputs ( $V_y$ ) is kept constant and the other one ( $V_x$ ) swept from  $-400$  mV to  $+400$  mV. By changing the constant voltage of  $V_y$  and then sweeping of  $V_x$ , desired outputs will be obtained. Within this range, the average of measured nonlinearity error is 0.94 %.

Tab. 1: Transistor aspect ratios.

Transistor name	W/L ( $\mu m/\mu m$ )
$M_1$ - $M_8$	10/0.18
$M_9$ - $M_{12}$	12/0.18
$M_{13}$ - $M_{16}$	4/0.18
$M_{17}$ - $M_{18}$	15/0.18

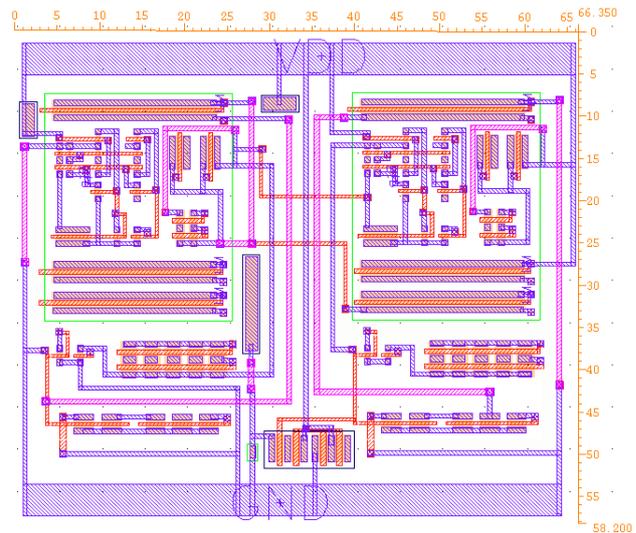


Fig. 2: Layout of the proposed multiplier circuit.

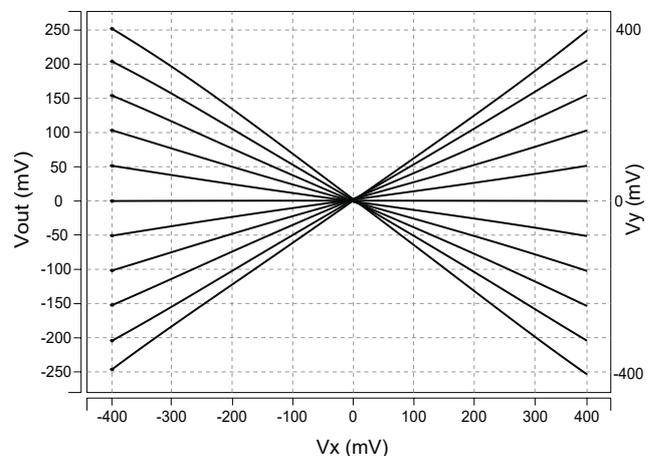
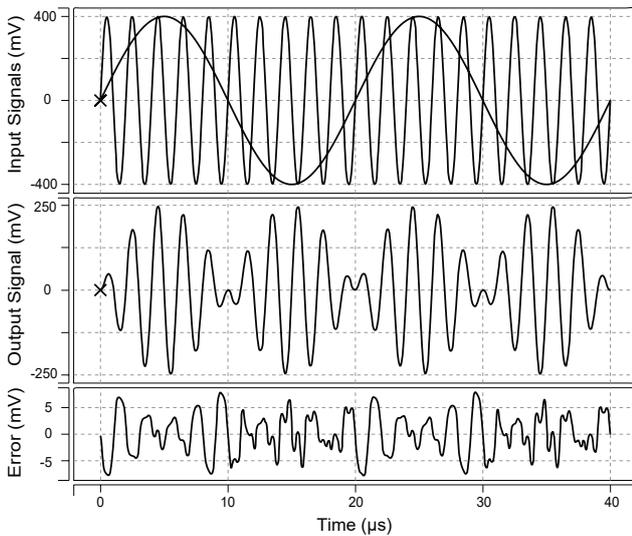
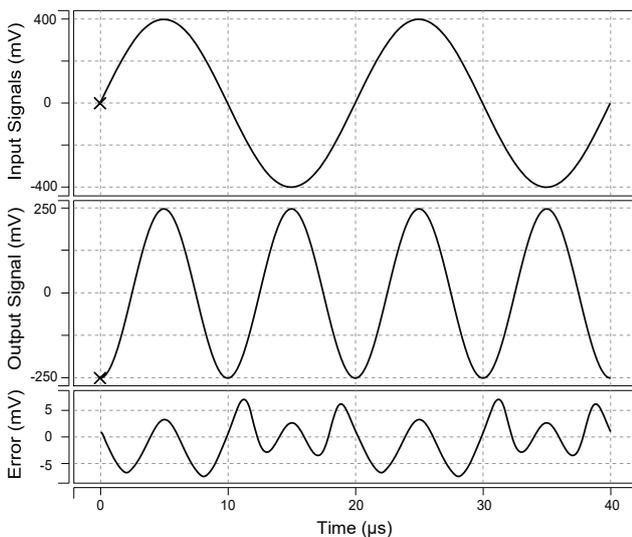


Fig. 3: Simulation result for DC transfer characteristic.

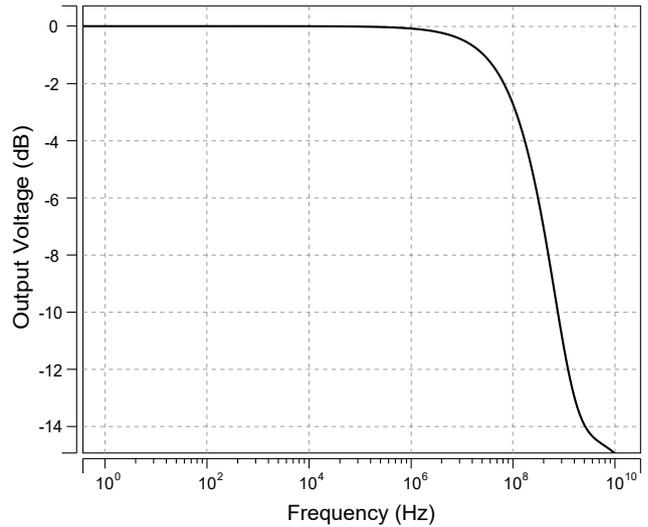
Figure 4 shows the multiplier being used for balance modulator as well as the error quantity.  $V_x$  and  $V_y$  are 500 kHz and 50 kHz, 800 mV<sub>P-P</sub> sinusoidal carrier and modulation signals, respectively fed to inputs of the proposed multiplier. Also Fig. 5 demonstrates how the multiplier circuit can be employed as a frequency doubler. In this simulation, if both frequencies of the input voltage are 500 kHz, the figure shows the corresponding output waveform with double frequency of 1 MHz. Frequency response in Fig. 6 shows that bandwidth of the circuit is 196 MHz when the input signal is applied to  $V_x$ , and  $V_y = 400$  mV. The same result is obtained for constant value of  $V_x$  and AC signals for  $V_y$ .



**Fig. 4:** Proposed multiplier as an amplitude modulator. 500 kHz carrier sinusoid and 50 kHz modulating signal (upper waveform); AC modulated output (middle waveform); Error measurement (lower waveform).

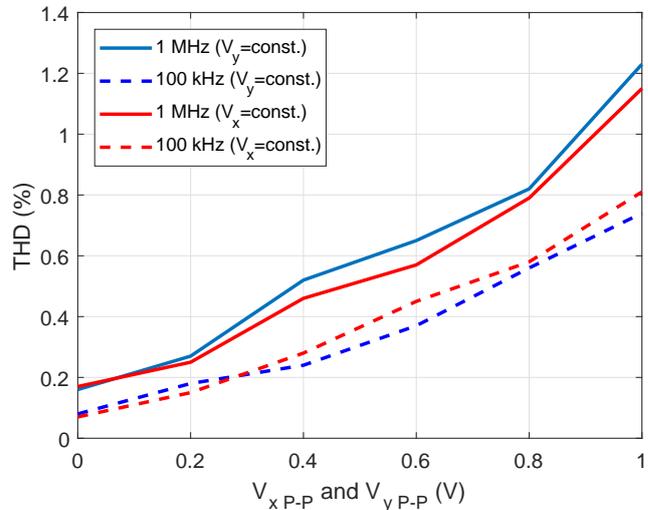


**Fig. 5:** The proposed multiplier as a frequency doubler, input signals (upper waveform); output signal (middle waveform); Error measurement (lower waveform).



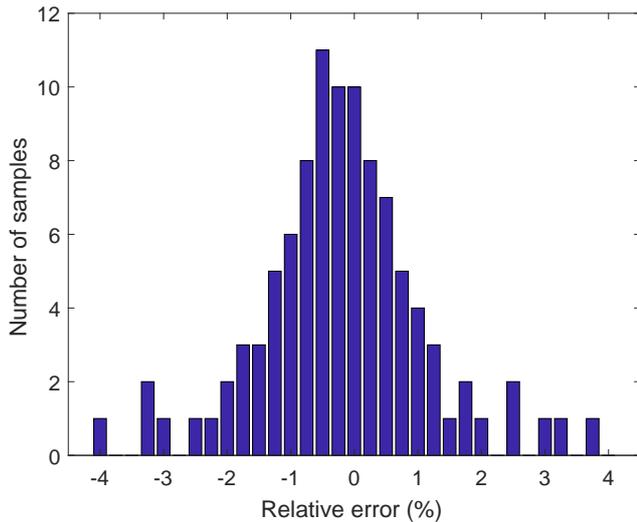
**Fig. 6:** Frequency response of the circuit.

The Total Harmonic Distortion (THD) versus input signal at 100 kHz and 1 MHz is shown in Fig. 7. THD simulations are carried out for both of  $V_x$  and  $V_y$ , when one of them is constant and another one is sinusoidal. In the worst case, an input signal of 1 V<sub>P-P</sub> at a frequency of 1 MHz resulted in a THD of less than 1.2 %.

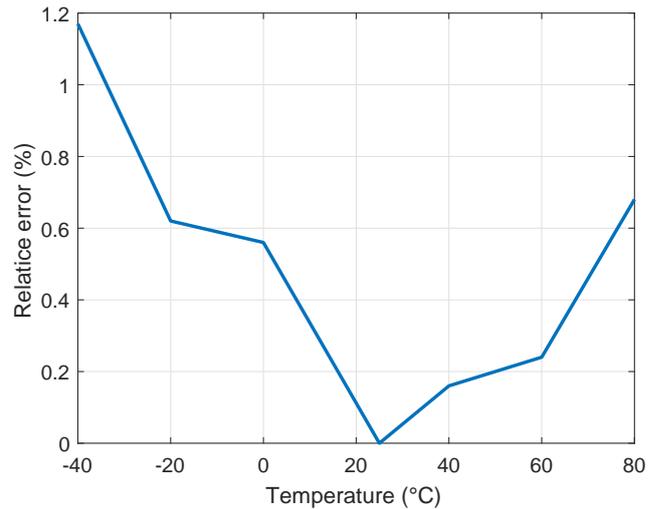


**Fig. 7:** Relation between THD,  $V_x$  and  $V_y$ .

In order to evaluate the robustness of the circuit against the process variation, the Monte Carlo analysis with 100 samples is performed by applying  $\pm 5\%$  Gaussian distribution at  $\pm 3\sigma$  level in the variation of all transistors aspect ratio and threshold voltage simultaneously. Two sinusoidal signals with the frequencies of 500 kHz and 1 MHz and also 400 mV<sub>P-P</sub> and 800 mV<sub>P-P</sub> amplitudes are applied to the circuit under the aforesaid variations and then the outputs are compared with the ideal values. The average of error in each sample is considered as the relative error. The



**Fig. 8:** Monte Carlo analysis of the circuit for  $\pm 5\%$  mismatch in threshold voltage and transistors aspect ratio.



**Fig. 9:** Relative error of the circuit versus different temperatures.

result is shown in Fig. 8, in which 68 % of the total samples occurred with the relative error of less than  $\pm 1\%$ .

To analyze the performance of the proposed circuit regarding temperature variations the simulations are carried out in different temperatures. The threshold voltage is the most important parameter in the analysis of temperature dependence of CMOS circuits [27]. Therefore, a small variation in threshold voltage causes a large change in the output. Although single-ended output of the squaring circuits (see Eq. (8) or Eq. (9)) includes the threshold voltage, the output of the complete circuit (see Eq. (12)) does not depend on the threshold voltage, therefore no remarkable change occurs at the final output.

Figure 9 shows the relative error of the circuit in different temperatures, where the maximum error occurred at  $-40\text{ }^\circ\text{C}$  with 1.18 %. In this simulation, the obtained output at the temperature of  $25\text{ }^\circ\text{C}$  is considered as the reference value (relative error = 0), then the resulted outputs in other temperatures are compared with that value and the relative error is computed. It should be pointed out that the input signals are the same as the signals that were applied in the Monte Carlo analysis. The characteristics of the circuit are

summarized in Tab. 2 and compared with the former works to prove the efficiency of the circuit.

## 5. Conclusion

A new CMOS voltage-mode analog multiplier circuit was presented in this paper. The key features of the circuit are its high accuracy and high linearity as well as its body effect-free operation, owing to the fact that the circuit was designed based on a new symmetrical configuration. Compared to the previously reported works, the dynamic input and output ranges of the circuit are considerably improved, since the circuit works in the saturation region not in weak inversion. To prove the efficiency of the proposed circuit, it was employed as a modulator and frequency doubler, and the simulation results were compared with ideal performance of these applications. The performance of the proposed multiplier was characterized using HSPICE with TSMC level 49 (BSIM3v3) parameters for  $0.18\text{ }\mu\text{m}$  CMOS technology.

**Tab. 2:** Comparative parameters of the proposed multiplier with other recent works.

	[9]	[10]	[22]	[24]	This work
Power supply (V)	0.5	1.5	1.4	1.5	1.5
Input range (mV)	$\pm 80$	$\pm 120$	$\pm 560$	$\pm 200$	$\pm 400$
Output range (mV)	$\pm 10$	$\pm 150$	$\pm 10\text{ }\mu\text{A}$	$\pm 2$	$\pm 250$
Power consumption ( $\mu\text{W}$ )	0.714	6.7	72.6	32	44
THD (%); 100 kHz, 400 mV	4.11	4.2	1.3	1.7	0.58
Nonlinearity (%)	5.6	3.2	1.9	5.3	0.94
-3 dB bandwidth (MHz)	0.221	0.268	249	1980	196
Tech. ( $\mu\text{m}$ )	0.18	0.35	0.25	0.35	0.18

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