# An Interline Dynamic Voltage Restorer Using Neutral-Point-Clamped (NPC) Multilevel Converter

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***Abstract.*** *Because of increased number of sensitive loads and automated processes in industry, need for high quality power is nowadays inevitable. Deteriorated power quality my result in huge financial losses and also decreases the productivity. The power electronic based solutions for improving power quality have become more common in the recent years. One of these solutions is to use the Dynamic Voltage Restorer (DVR), which is a series-connected voltage compensator. Interline DVR (IDVR) is a special structure, in which two DVRs share a DC-link. These two DVRs are installed in two independent distribution feeders which may have two different voltage levels. In this paper, a new structure for IDVR is proposed. The proposed DVR is based on the multilevel converters. Therefore, we call it as Multilevel Converter based IDVR (MLC-IDVR). Because of using multilevel converter, the quality of voltage waveform in the proposed structure is improved in comparison with the conventional IDVR. Also, it is more suitable for higher voltage applications. The performance of the proposed MLC-IDVR is verified by simulation results carried out by PSCAD/EMTDC software.*

## Keywords

***Dynamic voltage restorer, multilevel converter, voltage sag.***

## 1. Introduction

Power quality has been one of the most investigated issues in the field over the past years. This is because of the fact that losses (financial and technical) due to bad quality of power are sometimes huge and in-compensable [1] and [2]. Besides the financial losses, the bad quality of power can put human life at risk in e.g. hospitals. Other reason behind the increased attention to power quality is the ever-increasing number of sensitive loads. Improper power quality usually results in failure or malfunction of the sensitive loads. Therefore, in highly automated industries the improper power quality can lead to loss of productivity [3]. Among the power quality problems, the voltage quality is the most common and most important to end users. Voltage quality includes various issues. However, the voltage sag defined as sudden decrease in the magnitude of voltage for a short period, is the most frequent and severe issue [4].

Different techniques are used in order to compensate for voltage sags. However, the most practical and economical solution is to use power-electronic converter based devices called custom power devices [5]. The custom power devices are available in different configurations. The series-connected custom power devices are well-suited for voltage sag compensation. These devices are called Dynamic Voltage Restorers (DVR) [6]. The DVR is simply a converter (usually Voltage Source Inverter (VSI)) supplied by an energy storage and connected in series to the grid using injection transformer. The VSI generates the required compensation voltage so that the load voltage remains almost unchanged when voltage sag occurs [7]. In fact, the DVR can be seen as a series-connected controlled voltage source [8]. However, many topologies and control strategies have been presented for the DVRs. Four system topologies are available for DVRs [9] that have their own advantages and shortcomings. Besides the system topologies, the VSI topologies that have been used in the DVR structure have a wide variety. The three-phase six switch inverter, H-bridge inverter, four-leg inverter, multilevel inverters, Z-source inverters and direct AC-AC converters are the common topologies used in the

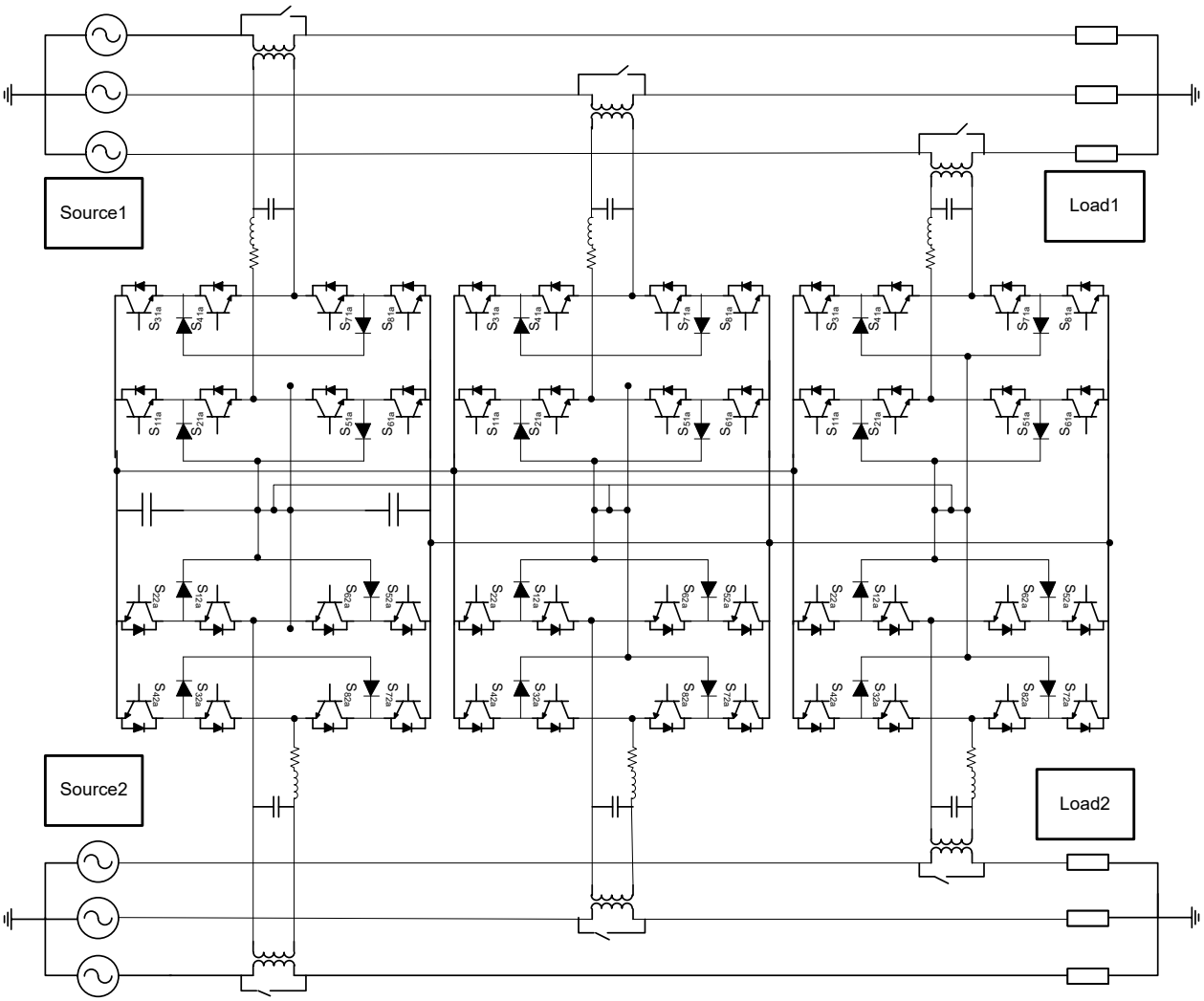



**Fig. 1:** The proposed multilevel converter based interline DVR.

DVR structure [10], [11], [12], [13] and [14]. A thorough review of the DVR can be found in [15].

As a kind of DVRs, the Interline DVR (IDVR) has also been reported in the literature [16], [17] and [18]. The IDVR provides a way to replenish the energy in the common DC-link energy storage dynamically. The IDVR system consists of several DVRs protecting sensitive loads in different distribution feeders emanating from different grid substations, and these DVRs share a common DC link. When one of the DVRs in IDVR system compensates for voltage sag by importing real power from the DC link, the other DVRs replenish the DC-link energy to maintain the DC-link voltage at a specific level. An example of a potential location for such a scheme is an industrial park where power is fed from different feeders connected to different grid substations, those that are electrically far apart. The sensitive loads in this park may be protected by DVRs connected to respective loads. The DC-links of these DVRs can be connected to a common terminal, thereby forming an IDVR system. This would cut down the cost of the custom-power device, as sharing common DC link reduces the size of the DC-link storage capacity substantially compared to that of a system, in which loads are protected by clusters of DVRs with separate energy storage systems [18]. Optimum design of IDVR has been investigated in [19]. Also a fast control scheme for IDVR has been presented in [20]. In [21], the cascaded H-bridge converter based IDVR is presented.

The application of multilevel converters in IDVRs has been rarely reported in the literature. Therefore, this paper focuses on the application of multilevel converter in the IDVR structure. In Sec. 2. , the proposed Multilevel Converter based IDVR (MLC-IDVR) is presented. Operation principle of the two DVRs forming the IDVR is also discussed. The proposed control method of the MLC-IDVR is presented in Sec. 3. In order to verify the operation and control of the proposed MLC-IDVR, the simulation results are presented in Sec. 4.

## 2. The Proposed MLC-IDVR

Figure 1 shows the proposed multilevel converter based interline DVR. The well-known topologies of multilevel converters including the Cascaded H-Bridge (CHB) and Neutral-Point-Clamped (NPC) multilevel converters can be used. In this paper, one H-Bridge NPC (HB-NPC) multilevel converter is used for each phase. The HB-NPC is a 5-level converter. Therefore, the proposed MLC-IDVR is based on the 5-level converter.

It is important to note that higher number of voltage levels can be obtained by cascading the 5-level converters. As shown in Fig. 1, the IDVR is composed of the two DVRs, namely DVR1 and DVR2 sharing a DC-link. Each of the two DVRs uses three 5-level HB-NPC converters, one per phase. As the converters are connected via a transformer, the DC-link of all of them can be shared. In other words, only one DC-link is required. An LC filter is used at the output of each converter to filter out the high-frequency components of the output voltage. Also, a bypass switch for each converter is used to bypass the DVR in normal condition of the grid. In order to better investigate the operation of the IDVR, suppose that the DVR1 operates in voltage sag compensation mode and DVR2 operates in regulating the DC-link voltage mode. Operation of the two DVRs in the mentioned modes is described in the following subsections.

### 2.1. Operation of DVR1

Three main compensation strategies are available for DVR; pre-sag method, in-phase method and energy optimization method [22]. As verified in [18], if the energy optimization method is used for compensation of voltage sags, the compensation capability of the DVR will increase and deeper voltage sags can also be compensated. Therefore, this method is used in this paper. Phasor diagram of the energy optimization compensation method is shown in Fig. 2. The principle of this method is to draw the lowest possible energy from the DC-link by increasing the angle between the line current and the injected voltage. This technique helps the DVR cope with deeper voltage sags.

Based on [23], when the line current is in-phase with the source voltage $V_{SI}$, the minimum power operation is achieved. In other words, for minimum power injection, $\gamma = 0$.

Considering Fig. 2, the value of $\sigma$ (current between the DVR1 output voltage and the pre-sag source voltage) can be obtained as follows:

$$\sigma = \tan^{-1}\left(\frac{V_{L1,m}\sin(\phi-\alpha)+V_{S1,m}\sin(\alpha)}{V_{L1,m}\cos(\phi-\alpha)-V_{S1,m}\cos(\alpha)}\right). \quad (1)$$

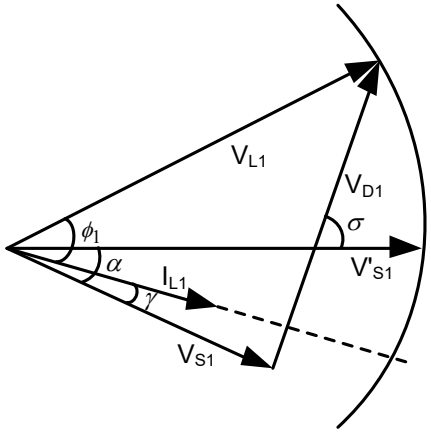



**Fig. 2:** Phasor diagram of the energy optimization compensation method.

The equation is used in the control procedure of the DVR1. The DVR1 output voltage will lead the pre-sag source voltage ($V'_{SI}$ ) by the phase angle of $\sigma$.

### 2.2. Operation of DVR2

As the task of DVR1 is considered to be voltage sag compensation, the task of DVR2 is therefore to charge the DC-link and provide the energy required for voltage sag compensation. The main point about the operation and control of DVR2 is that its output voltages should be in a way (in terms of magnitude and phase angle) that the downstream load of the corresponding feeder do not experience any change in the magnitude of voltage. Taking this point in mind, the phasor diagram of DVR2 is shown in Fig. 3. As this figure shows, the magnitude of sum of the corresponding source voltage and DVR2 voltage is 1 per-unit. This should always be taken into account to control the DVR, which have the duty of charging the DC-link. In order to calculate the power transferred to DC-link by DVR2 ($P_{D2}$), the phase angle between DVR2 output voltage ($V_{D2}$) and line2 current ($I_{L2}$) should be determined. Considering Fig. 3, it can be written as follows:

$$\delta = 180 - \left(\frac{180-\beta}{2}\right) + (\phi_2 - \beta) = 90 - \frac{\beta}{2} + \phi_2, \quad (2)$$

where, $\delta$ is the phase angle between $V_{D2}$ and $I_{L2}$.

The power transferred to DC-link by DVR2 can be calculated as follows:

$$\begin{aligned} P_{D2} &= V_{D2,rms}\cdot I_{L2,rms}\cos(\delta), \\ &= V_{D2,rms}\cdot I_{L2,rms}\cos(90-\frac{\beta}{2}+\phi_2), \\ &= V_{D2,rms}\cdot I_{L2,rms}\sin(\frac{\beta}{2}-\phi_2), \\ &= \frac{V_{D2,m}\cdot I_{L2,m}}{2}\sin(\frac{\beta}{2}-\phi_2). \end{aligned} \quad (3)$$

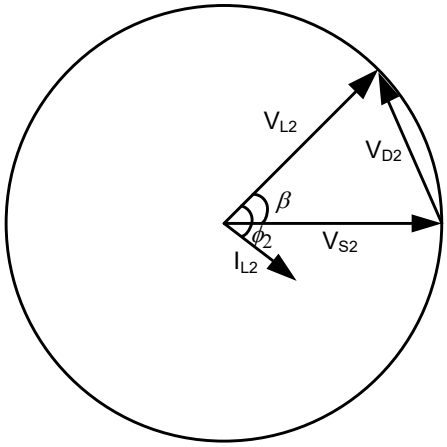



**Fig. 3:** Phasor diagram of DVR2.

The magnitude of source and load on feeder2 are equal:

$$V_{L2,m} = V_{S2,m} = V_m. \tag{4}$$

Using Eq. (4) and considering Fig. 3, the following equation can be obtained:

$$V_{D2,m} = \\ = 2V_m \cdot \cos\left(\frac{180-\beta}{2}\right) = 2V_m \cdot \sin\left(\frac{\beta}{2}\right). \tag{5}$$

# 3. Control Method

The control methods of the two DVRs are described in the following sections. It should be noted that the DVR1 operates in voltage sag compensation mode. It uses the well-known control methods. The DVR2 operates in DC-link charging mode. Its operation is based on the simple equation obtained in the previous section.

## 3.1. Control Method of DVR1

As mentioned, DVR1 operates in voltage sag compensation mode. Because of the fact that there is a limitation in active power, the minimum energy compensation strategy is selected for DVR1. The basics of this compensation strategy have been described in previous section. The phase angle of the DVR1 output voltage has been calculated before (see Eq. (1)). However, its magnitude should also be calculated. Considering Fig. 2, the magnitude of DVR1 output voltage ($V_{D1,m}$) can be obtained as follows:

$$V_{D1,m} = \sqrt{{V_{L1,m}}^2 + {V_{S1,m}}^2 - 2V_{L1,m}V_{S1,m}\cos(\phi_1)}. \tag{6}$$

As the magnitude and phase angle of the DVR1 output voltage is determined, its control is straight forward. Figures 4 shows the control block diagram of DVR1. It is simply a synchronous reference frame vector control. However, the dq to abc transform leads the abc to dq transform by the phase angle equal to $\alpha + \sigma$. This is adopted to implement the minimum energy compensation strategy (see Fig. 2 where $V_{D1}$ leads $V_{S1}$ by $\alpha + \sigma$). As the reference waveforms are generated, the Level-Shifted Pulse-Width-Modulation (LS-PWM) method is used to provide the switching pulses. This PWM method is most suited for the NPC multilevel inverters [24].

## 3.2. Control Method of DVR1

DVR2 operates in DC-link charge mode. Considering Eq. (3), the power drawn from feeder2 by DVR2 depends on $\beta$. Therefore, in control system, $\beta$ is determined by a Proportional-Integral (PI) controller applied to the error between the measured and reference values of the DC-link voltage. As $\beta$ is determined, the magnitude of DVR output voltage ($V_{D2,m}$) can be calculated using Eq. (5). Consequently, both phase angle and magnitude of DVR2 output voltage are determined. It should be noted that the phase angle of DVR2 output voltage in reference to the source voltage is equal to $\frac{\pi+\beta}{2}$ (see Fig. 3). The control system of DVR2 is simply shown in Fig. 5.

# 4. Simulation Results

This section verifies the proposed MLC-IDVR topology and the adopted control method by simulation results. The results are obtained in the PSCAD software environment. The main data of system are given in Tab. 1. The simulation results are presented for two different voltage sag conditions; balanced three-phase voltage sag and unbalanced single-phase voltage sag.

**Tab. 1:** Main data of the simulation system.

| Parameter | Value |
|---|---|
| Nominal voltage of system (phase to neutral RMS) | 220 V |
| System frequency | 50 Hz |
| Switching frequency | 1500 Hz |
| Load1 | 35+j17 ohm |
| Load2 | 20+j15 ohm |
| DC-link reference voltage | 200 V |
| Each DC-link capacitor | 5000 μF |
| Filter components (LC) | 2 mH, 45 μF |
| Injection transformers (ratio, inductance) | 1:1, 0.9 mH |

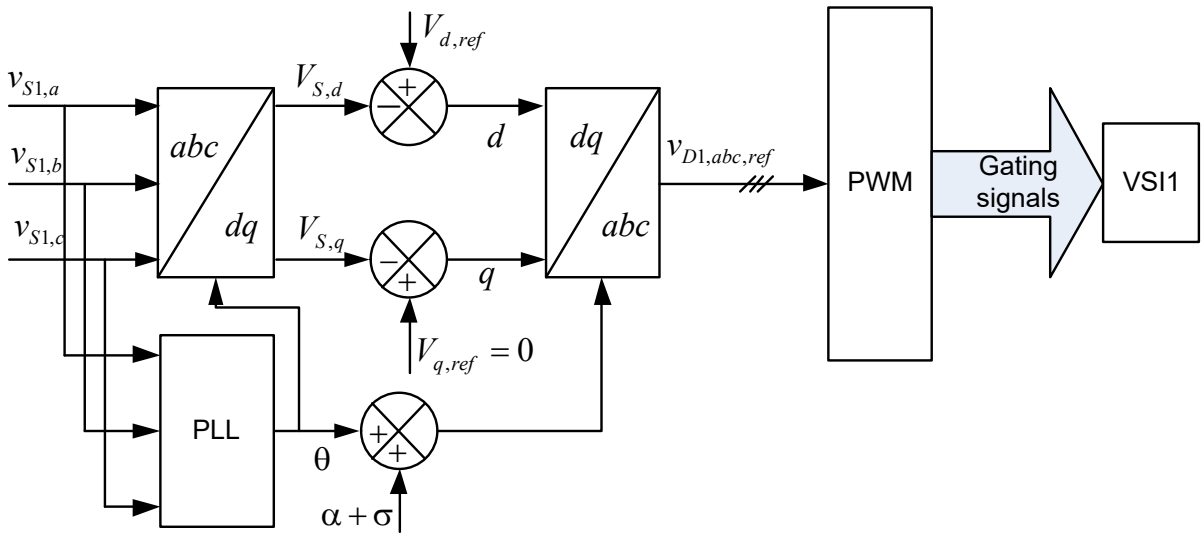



**Fig. 4:** Control block diagram of DVR1.

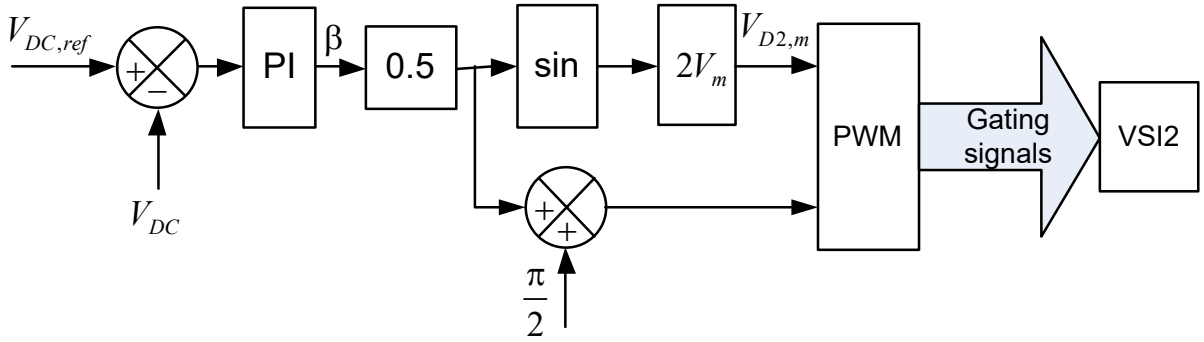


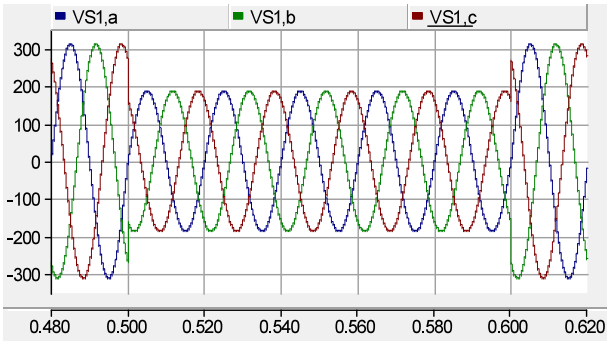

**Fig. 5:** Control block diagram of DVR2.

### 4.1. Results for the Balanced Three-Phase Voltage Sag

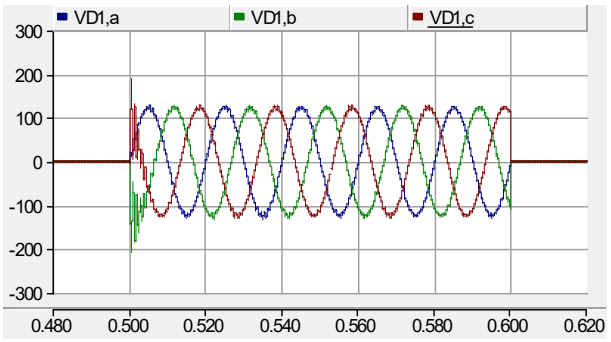
In this condition, the voltage sag occurs on all three phases and the value of sag is equal for all phases. The value of voltage sag is assumed to be 0.4 pu in reference to the nominal source voltage. In other words, the Root-Means-Square (RMS) value of phase voltages drops to 132 V from 220 V. It should be noted that the voltage sag occurs on feeder1, and feeder2 is not affected by the voltage sag.

The source voltage of the feeder1 is shown in Fig. 6(a). As the figure shows, the voltage starts at 0.5 s and ends at 0.6 s. Figure 6(b) shows the DVR1 output voltage. As this figure indicates, when the voltage sag occurs, DVR1 generates and injects proper compensation voltage. The magnitude and phase angle of the DVR1 output voltage is in a way that the load voltage is fully compensated. The compensated load voltage is shown in Fig. 6(c). As this figure shows, the full compensation is achieved. The Total Harmonic Distortion (THD) of the DVR1 and load1 voltage is 2.31 %, and 0.92 %, respectively. For a three-level H-bridge inverter based IDVR (keeping other conditions constant), the corresponding values of THD are 21.14 % and 8.44 %, respectively. Because of using the 5-level inverter, the THD of the output waveforms is much lower in the proposed IDVR. The output voltage of DVR1 in phase a before the filter is shown in Fig. 7. This figure verifies that the 5-level inverter is used.

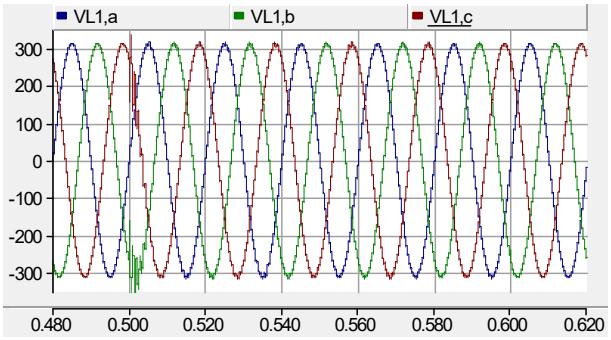
The voltage sag compensation is achieved by taking the required energy from feeder2. The value of source voltage on feeder2 is shown in Fig. 8(a). This figure indicates that there is no voltage sag on feeder2. The DVR2 charges the DC-link by taking energy from feeder2 and delivering it to the DC-link. This is achieved by injecting of a proper three-phase voltage to feeder2. The DVR2 output voltage is shown in Fig. 8(b). The DVR2 output voltage should be in a way that the DC-link voltage is supported and also the magnitude of load2 voltage remains unchanged. The load2 voltage is shown in Fig. 8(c). As the figure shows, when the voltage sag occurs on feeder1, the phase angle of




(a) Source voltage.

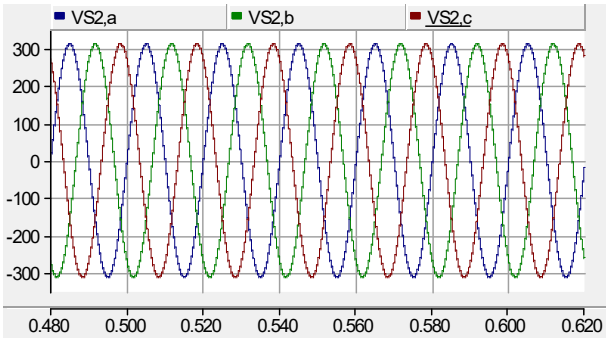



(b) DVR1 output voltage.

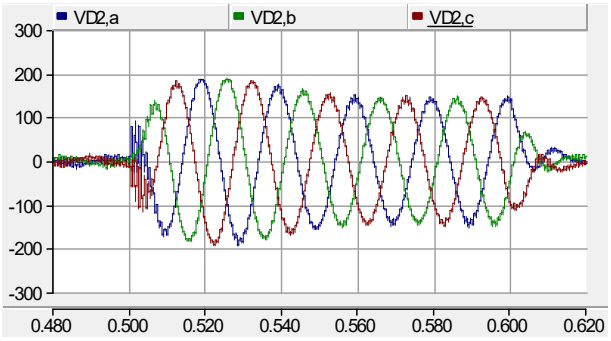



(c) Load1 voltage.

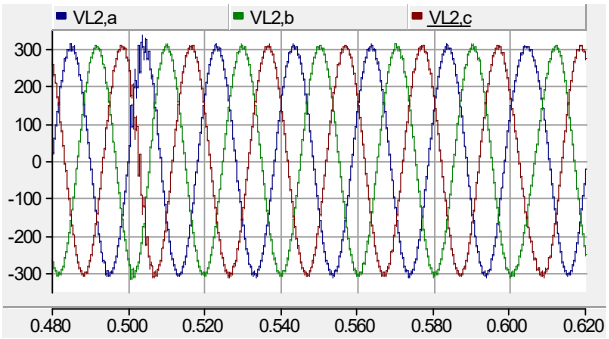
**Fig. 6:** Performance of DVR1 in balanced voltage sag compensation.




(a) Source voltage.




(b) DVR2 output voltage.




(c) Load2 voltage.

**Fig. 8:** Performance of DVR2 in unbalanced voltage sag compensation.

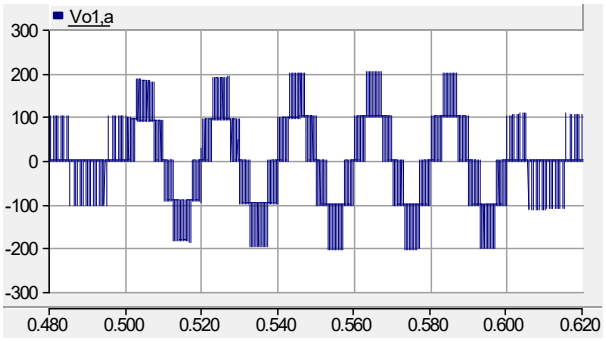



**Fig. 7:** Output voltage of DVR1 in phase a before filter.

load2 voltage changes slightly. This is necessary for providing the active power needed for compensation. The THD of the DVR2 output voltage and that of the corresponding load voltage is 3.57 % and 1.65 %, respectively. For the conventional H-bridge based IDVR, the corresponding THD values are 13.73 % and 7.51 %, respectively. Figure 9 Shows the output voltage of DVR2 before the filter in phase a. as this figure shows, the 5-level converter is used.

The main aim of DVR2 is to regulate the DC-link voltage. The DC-link voltage is shown in Fig. 10. As the figure shows, the DC-link voltage is regulated properly. However, there are slight changes in the start and end instants of voltage sag. This is natural and is due to the time constant of a control system.

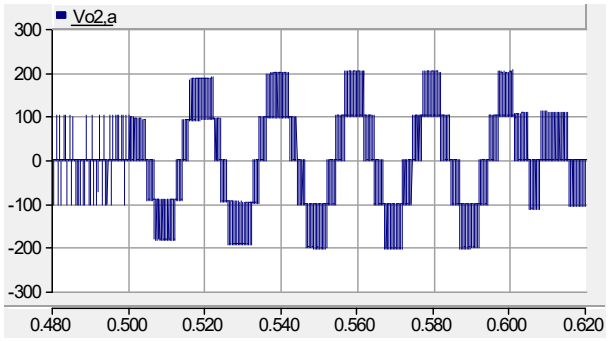



**Fig. 9:** Output voltage of DVR2 in phase a before filter.

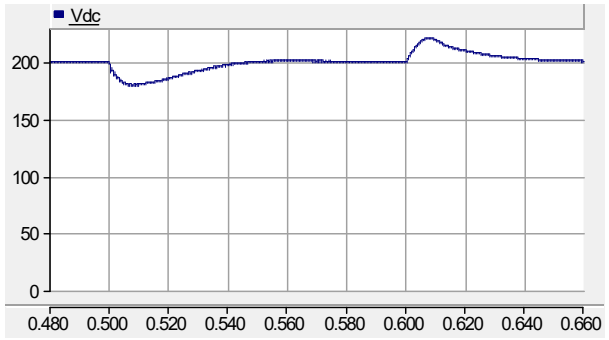


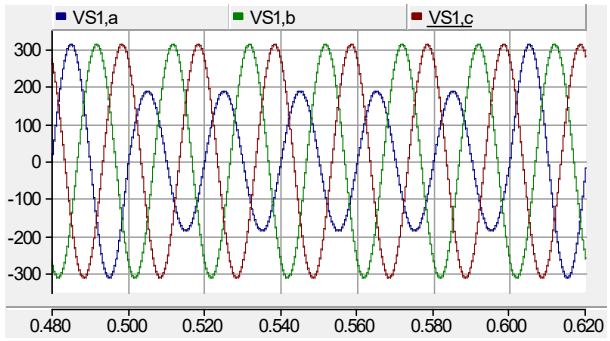

**Fig. 10:** DC-link voltage in balanced voltage sag condition.

## 4.2. Results for the Balanced Three-Phase Voltage Sag

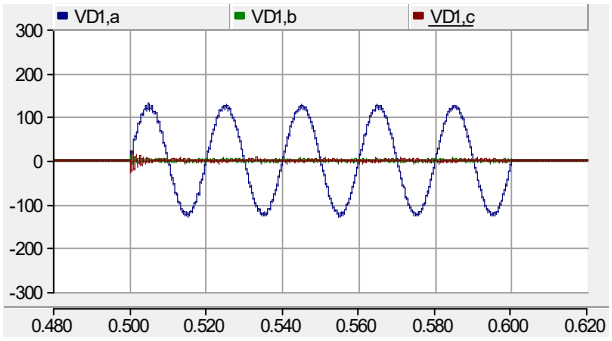
The unbalanced voltage sag, defined in three-phase systems, is a voltage sag, in which the sag characteristic are not the same for all of the phases. There are many types of unbalanced voltage sags. However, the most common unbalanced voltage sag is the single-phase sag where the voltage sag occurs in one of the phases. Therefore, the single-phase voltage sag is considered for performance evaluation of the IDVR.

Figure 11(a) shows the source voltage on feeder1 where the 0.6 pu single-phase voltage sag (in phase a) can be observed. It starts at 0.5 s and ends 0.6 s. Figure 11(b) shows the DVR1 output voltage. As this figure shows, in the phase a where voltage sag is applied, DVR1 generates the proper compensating voltage. In the other two phases, the voltage in sag period is negligible. Figure 11(c) shows the compensated load voltage. The THD value of the DVR1 output voltage and the load voltage is 2.38 %, 0.95 %, respectively.

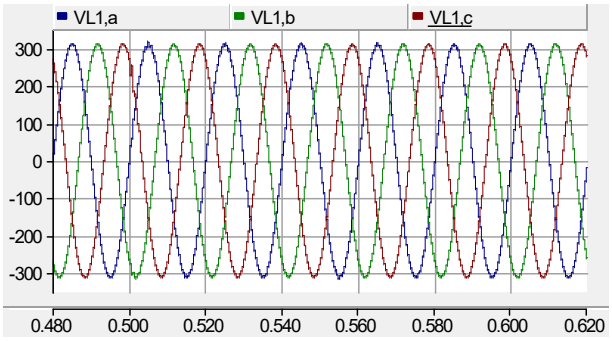
DVR2 operates as a DC-link charger. The source voltage on feeder2 is shown in Fig. 12(a). It is noticeable that there is no voltage sag on feeder2. The DVR2 output voltage is shown in Fig. 12(b). The DVR2 generates and injects a set of three-phase voltages with such a magnitude and phase angle that the DC-link voltage is regulated and also the magnitude of load2 voltage remains constant. Load2 voltage is shown in




(a) Source voltage.




(b) DVR1 output voltage.




(c) Load1 voltage.

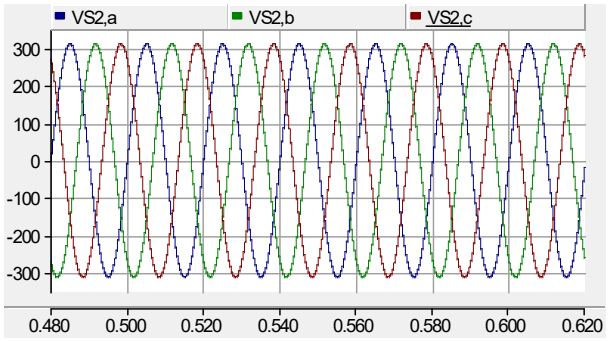
**Fig. 11:** Performance of DVR1 in unbalanced voltage sag compensation.

Fig. 12(c), in which the magnitude is constant. The DVR2 output voltage and the load2 voltage THD is 8 % and 1.1 %, respectively.

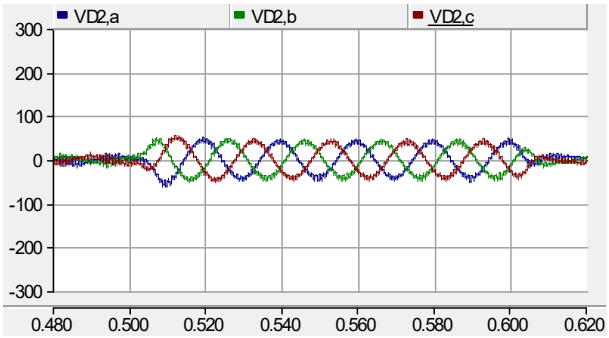
The DC-link voltage is shown in Fig. 13. Despite slight variations at the start and end instants of the voltage sag, the DC-link voltage is constant verifying the satisfactory operation and control of DVR2.

## 4.3. Results for a 10 kV System

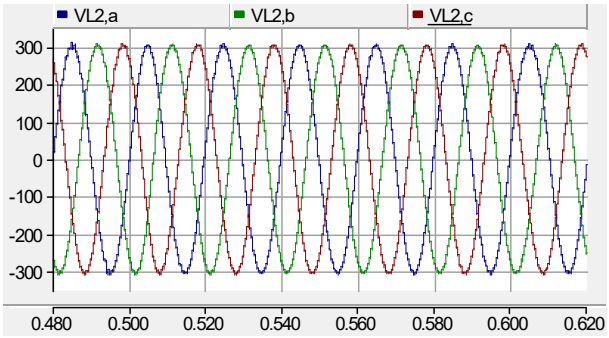
In order to study the performance of the IDVR in higher voltage levels, a simulation is done on a 10 kV system (RMS line voltage of a three-phase system). Other data of the simulated system are as given Tab. 1. In order to have different simulation studies, unbal-




(a) Source voltage.




(b) DVR2 output voltage.




(c) Load2 voltage.

**Fig. 12:** Performance of DVR1 in unbalanced voltage sag compensation.

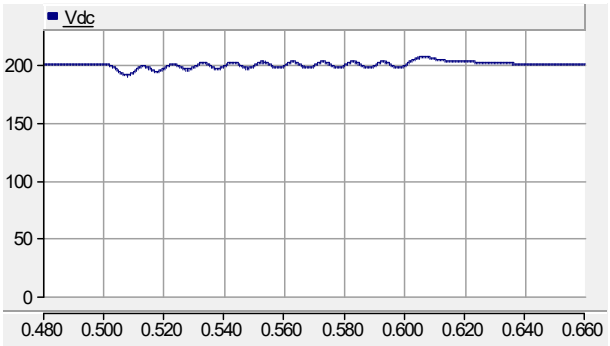



**Fig. 13:** DC-link voltage in unbalanced voltage sag condition.

anced two-phase voltage sag of 51 % is considered for the 10 kV system. The simulation results of the 10 kV IDVR are shown in Fig. 14 and Fig. 15. Figure 14 indicates the simulation waveforms of the DVR1. In this figure, the source voltage, DVR1 output voltage and the corresponding load voltage waveforms are indicated from top to bottom of the figure, respectively. As the figure indicates, the two-phase voltage sag occurs and the DVR generates the required compensating voltage in the corresponding phases, as a result, the voltage of the load is fully restored to its nominal condition. The THD value of the DVR1 output voltage and the load voltage is 2.57 % and 1.1 %, respectively. The performance of the DVR2 is indicated in Fig. 15. In this figure, the corresponding source voltage, DVR output voltage, load voltage and also the DC-link voltage are presented. the source voltage has no sag and therefore, DVR2 operates to regulate the DC-link voltage. This is done by injecting a set of three-phase voltages with proper magnitude and phase angle to keep the load voltage magnitude constant and transfer active power to the DC-link and regulate its voltage. The THD value of the DVR2 output voltage and the corresponding load voltage is 7.03 % and 2.59 %, respectively.

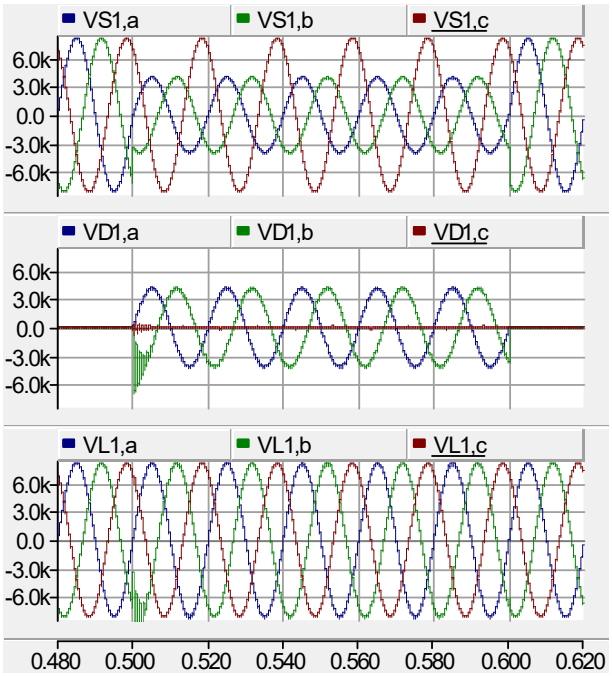



**Fig. 14:** Performance of DVR1 in 10 kV system and unbalance voltage sag, from top to bottom the waveforms are: source voltage, DVR1 output voltage, and load1 voltage.

In order to compare the results of the proposed IDVR with those of a conventional IDVR, an IDVR based on three-level H-bridge inverter (one H-bridge for each phase) has also been simulated in the same condition. For the three-level H-bridge based IDVR, the THD value of the DVR1 output voltage and the corresponding load voltage is obtained as 9.3 %, 18 %, respectively. Also, the THD value of the DVR2 output

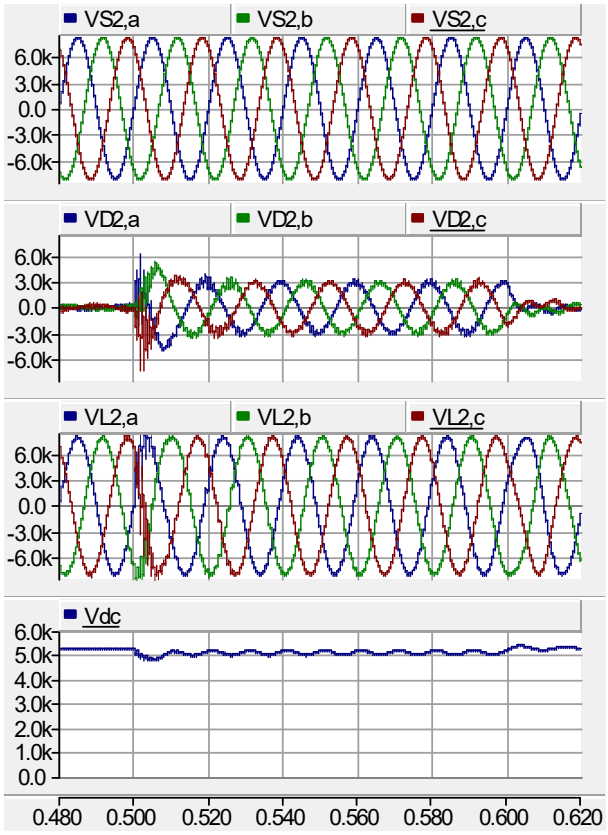



**Fig. 15:** Performance of DVR2 in 10 kV system and unbalance voltage sag, from top to bottom the waveforms are: source voltage, DVR2 output voltage, and load2 voltage, and DC-link voltage.

voltage and the corresponding load voltage is obtained as 8.6 %, 13.8 %, respectively. The results indicated that the quality of the output waveforms in the proposed IDVR is considerably higher than those of the conventional topology.

## 5. Conclusion

The Multilevel Converter based Interline Dynamic Voltage Restorer (MLC-IDVR) is proposed in this paper. In the proposed structure, the multilevel converters are used. In this study, the CHB-NPC multilevel converter is used. However, other topologies of multilevel converters can also be used. Because of using multilevel converters, the output voltage quality is improved and also the output filter size is reduced. Suitable control methods to control both DVRs of the IDVR have been discussed. Performance of the proposed MLC-IDVR has been examined by simulations carried out using PSCAD software. The results have been obtained in two voltage sag conditions (balanced three-phase and unbalanced single-phase voltage sag). The satisfactory operation of the MLC-IDVR in compensating the voltage sags and regulating the DC-link voltage has been verified by the results.

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