Load Insensitive, Low Voltage Quadrature Oscillator Using Single Active Element

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Abstract. *In this paper, a load insensitive quadrature oscillator using single differential voltage dual-X second generation current conveyor operated at low voltage is proposed. The proposed circuit employs single active element, three grounded resistors and two grounded capacitors. The proposed oscillator offers two load insensitive quadrature current outputs and three quadrature voltage outputs simultaneously. Effects of non-idealities along with the effects of parasitic are further studied. The proposed circuit enjoys the feature of low active and passive sensitivities. Additionally, a resistorless realization of the proposed quadrature oscillator is also explored. Simulation results using PSPICE program on cadence tool using 90 nm Complementary Metal Oxide Semiconductor (CMOS) process parameters confirm the validity and practical utility of the proposed circuit.*

Keywords

Load insensitive, quadrature oscillator, resistorless.

1. Introduction

Nowadays, research in analog signal processing has gone in the direction of low-voltage and low-power design. In addition, many new applications continue to emerge where new analog topologies have to be designed to ensure the trade-off between power and speed requirements. Finally, the modern development towards miniaturized circuits has given a strong and significant enhancement towards the implementation of low-voltage and low-power analog circuits. Ever since the introduction of analog signal processing, the need of new active devices has always been very significant. Recently, with the increasing demand of low-voltage and low-power circuits, current conveyors have achieved popularity [1], [2] and [9]. With the use of current conveyors, a number of applications can be realized such as: differentiators, integrators, impedance simulators, impedance converters, biquadratic filters, instrumentation amplifiers, oscillators, etc. The realizations of oscillators using different variation of current conveyors have received significant attention due to their numerous advantages. In the literature a number of quadrature oscillators based on different active elements are also reported. The quadrature oscillators in [3], [4], [5] and [6] produced voltage-mode signals and the ones in [7], [8], [9], [10] and [11] produced current-mode signals. Although some of the quadrature oscillators in [12], [13], [14] and [15] generated both voltage-mode signals as well as current-mode signals. Moreover, few of them are based on single active element [7], [8], [10] and [15].

The idea behind this paper is to propose a new load insensitive, low voltage quadrature oscillator using a single Differential Voltage Dual-X Second generation Current Conveyor (DV-DXCCII) along with five grounded passive components (three grounded resistors and two grounded capacitors). The proposed circuit design offers many advantages such as the use of single active element, the use of all grounded passive components, operated at low voltage, simultaneous availability of quadrature voltage and load insensitive quadrature current outputs, low active and passive sensitivities and resistorless realization.

2. Proposed Circuit

Differential Voltage Dual-X second generation Current Conveyor (DV-DXCCII) is an analogue building block [16] which is characterized by Eq. (1).

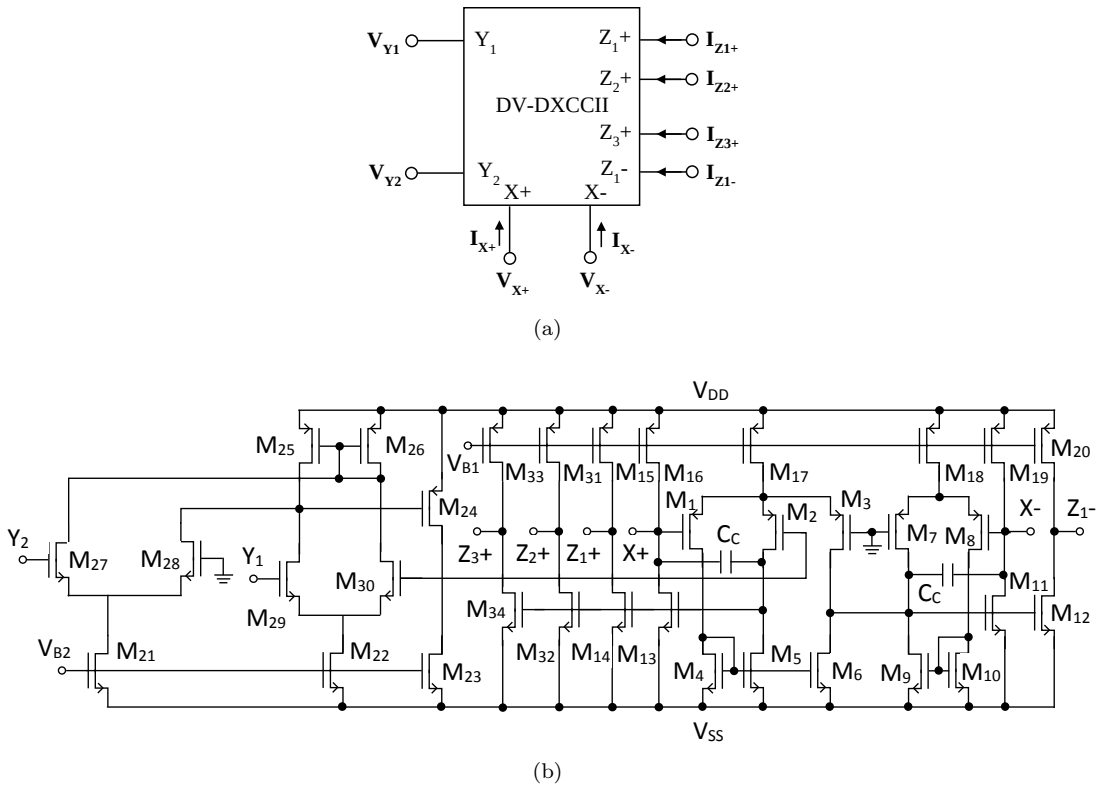


Fig. 1: (a) Schematic Symbol of DV-DXCCII (b) CMOS realization of DV-DXCCII [16].

The schematic symbol and CMOS realization of DV-DXCCII are shown in Fig. 1, where the CMOS realization comprises of Differential Voltage Current Conveyor (DVCC), i.e. M_{21} - M_{30}, with unused Z stages and dual-X second generation current conveyor (DXCCII), i.e. M_1 – M_{20}. In the realization of DV-DXCCII, X terminal of DVCC will drive the Y terminal of the DXCCII. The output terminals Z_{1+} and Z_{1-} are realized from the joint drains of M_{14}, M_{15} and M_{12}, M_{20} transistors, respectively. The features of both DVCC [2] and DXCCII [9] are combined together in this single active element. However, additional Z+ stages (Z_{2+} and Z_{3+}) have been implemented by taking the extra cascaded structures of transistors (M_{31} – M_{32} and M_{33} – M_{34}).

$$\begin{bmatrix} \mathbf{I}_{Y1} \\ \mathbf{I}_{Y2} \\ \mathbf{V}_{X+} \\ \mathbf{V}_{X-} \\ \mathbf{I}_{Z1+} \\ \mathbf{I}_{Z2+} \\ \mathbf{I}_{Z3+} \\ \mathbf{I}_{Z1-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ -1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \mathbf{V}_{Y1} \\ \mathbf{V}_{Y2} \\ \mathbf{I}_{X+} \\ \mathbf{I}_{X-} \end{bmatrix}. \quad (1)$$

The proposed circuit of load insensitive, low voltage quadrature oscillator is shown in Fig. 2. The proposed circuit employs a single DV-DXCCII, three grounded resistors, and two grounded capacitors. The proposed oscillator provides two quadrature current outputs and three quadrature voltage outputs simultaneously. Since both the current outputs (I_{O1} and I_{O2}) are directly available at the high output impedance terminals (Z_{1-} and Z_{3+}) without any load thus the proposed circuit enjoys the benefit of load insensitive current outputs. The characteristic equation of the proposed quadrature oscillator using Eq. (1) is given as:

$$s^2 + s\left[\frac{1}{C_1R_1} + \frac{1}{C_2R_2} - \frac{1}{C_1R_2}\right] + \frac{1}{C_1C_2R_1R_2} = 0. \quad (2)$$

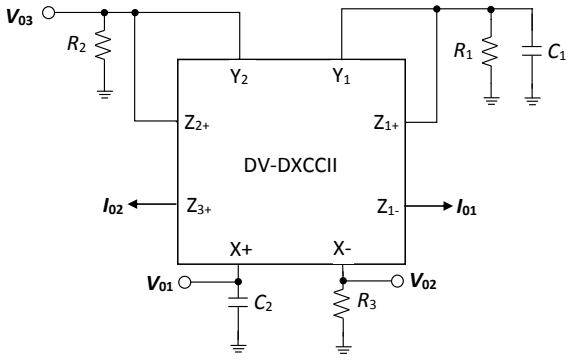


Fig. 2: Proposed load insensitive, low voltage quadrature oscillator.

Condition of Oscillation (CO) is given as:

$$CO: \frac{1}{C_1R_1} + \frac{1}{C_2R_2} \geq \frac{1}{C_1R_2}, \tag{3}$$

and the expression of Frequency of Oscillation (FO) is given as:

$$FO: \omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_2}}. \tag{4}$$

The phasor diagrams for the three quadrature voltage outputs (V_{O1}, V_{O2}, and V_{O3}) and two quadrature current outputs (I_{O1} and I_{O2}) are shown in Fig. 3(a) and Fig. 3(b), respectively. The three voltage and two current outputs of Fig. 3 are related as:

$$V_{O3} = j\omega C_2R_2V_{O1}, V_{O1} = -V_{O2}, \tag{5}$$

$$I_{O2} = -j\omega C_2R_3I_{O1}. \tag{6}$$

It is apparent from Eq. (5) and Eq. (6) that all the voltage and current outputs are in quadrature relationship.

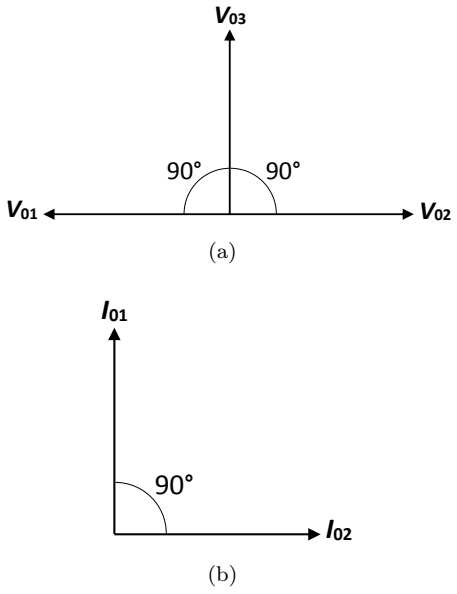


Fig. 3: Phasor diagram depicting (a) quadrature voltage relationship (b) quadrature current relationship.

3. Non-Ideal Analysis

By considering the non-ideal voltage and current transfer gains (α_i, where $i = 1, 2$ and β_j, where $j = 1, 2, 3, 4$) of DV-DXCCII, the modified voltage and current terminals relationship can be rewritten as:

$$\begin{bmatrix} \mathbf{I}_{Y1} \\ \mathbf{I}_{Y2} \\ \mathbf{V}_{X+} \\ \mathbf{V}_{X-} \\ \mathbf{I}_{Z1+} \\ \mathbf{I}_{Z2+} \\ \mathbf{I}_{Z3+} \\ \mathbf{I}_{Z1-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & 0 & 0 \\ -\beta_3 & \beta_4 & 0 & 0 \\ 0 & 0 & \alpha_1 & 0 \\ 0 & 0 & \alpha_2 & 0 \\ 0 & 0 & \alpha_3 & 0 \\ 0 & 0 & 0 & \alpha_4 \end{bmatrix} \begin{bmatrix} \mathbf{V}_{Y1} \\ \mathbf{V}_{Y2} \\ \mathbf{I}_{X+} \\ \mathbf{I}_{X-} \end{bmatrix}. \tag{7}$$

Here, β_1 and β_2 are the voltage transfer gains from Y_1 and Y_2 terminals, respectively to the X+ terminal. Similarly β_3 and β_4 are the voltage transfer gains from Y_1 and Y_2 terminals, respectively to the X− terminal. α_1, α_2, α_3 are the current transfer gains from X+ terminal to Z_{1+}, Z_{2+}, Z_{3+} terminals, respectively. α_4 is the current transfer gain from X− terminal to Z1− terminal. The ideal value of these voltage and current transfer gains is unity depending upon selected operating frequency.

Using Eq. (7), the proposed quadrature oscillator is reanalyzed. The non-ideal characteristic equation is obtained as:

$$s^2 + s\left[\frac{1}{C_1R_1} + \frac{1}{\alpha_2\beta_2C_2R_2} - \frac{\alpha_1\beta_1}{\alpha_2\beta_2C_1R_2}\right] + \\ + \frac{1}{\alpha_2\beta_2C_1C_2R_1R_2} = 0. \tag{8}$$

The non-ideal CO and FO are given as:

$$CO: \frac{1}{C_1R_1} + \frac{1}{\alpha_2\beta_2C_2R_2} \geq \frac{\alpha_1\beta_1}{\alpha_2\beta_2C_1R_2}, \tag{9}$$

$$FO: \omega_0 = \sqrt{\frac{1}{\alpha_2\beta_2C_1C_2R_1R_2}}. \tag{10}$$

The active and passive sensitivities with respect to ω_0 are given below

$$S^{\omega_0}_{\alpha_2,\beta_2} = S^{\omega_0}_{C_1,C_2,R_1,R_2} = -\frac{1}{2}, \quad S^{\omega_0}_{\alpha_1,\beta_1} = 0. \tag{11}$$

Equation (11) shows that the active and passive sensitivities with respect to frequency of oscillation are within unity in magnitude. Therefore, the proposed quadrature oscillator enjoys good active and passive sensitivity performance.

4. Parasitic Study

The performance of the proposed quadrature oscillator by considering the effects of various parasitic of DV-DXCCII is explored in this section. The parasitic model of DV-DXCCII is shown in Fig. 4, which

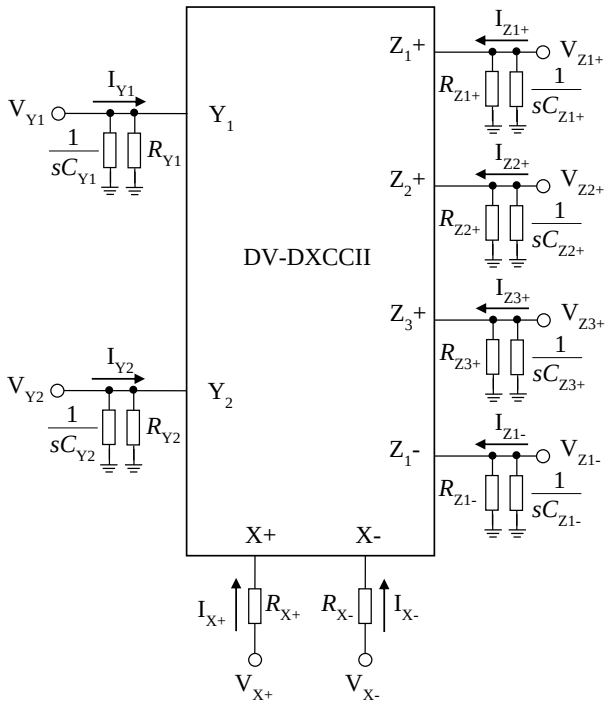


Fig. 4: The parasitic model of DV-DXCCII.

shows various ports parasitic. These various parasitic are port Y parasitic in the form of $R_Y//1/(sC_Y)$, port Z parasitic in the form of $R_Z//1/(sC_Z)$, and port X parasitic in the form of R_X. It is also worth mentioning that in the non-ideal case the parasitic resistances and capacitances appearing at the high input impedance terminal (Y) and high output impedance terminal (Z) are absorbed into the external grounded resistors and grounded capacitors as they are shunt with them. Thus, all grounded passive components based circuits are more suitable for monolithic integration. Moreover, the parasitic resistances at low impedance terminals (X+ and X−) are negligible (ideally they are zero). The parasitic impedances appearing at the X terminals would be connected between virtual grounds and actual ground and thereby eliminating their effect. However, the circuit with only capacitor at X terminal would show performance deterioration at higher frequencies [17]. In practice, to alleviate the effects of the parasitic impedances, the impedances should be chosen as:

$$Z_1 = \frac{1}{sC_1'}//R_1',$$

where:

$$R_1' = R_1//R_{Y1}//R_{Z1+},$$
$$\frac{1}{sC_1'} = \frac{1}{sC_1}//\frac{1}{sC_{Y1}}//\frac{1}{sC_{Z1+}},$$
$$Z_2 = \frac{1}{sC_Y}//R_2', \quad (12)$$

where:

$$R_2' = R_2//R_{Y2}//R_{Z2+},$$
$$\frac{1}{sC_Y} = \frac{1}{sC_{Y2}}//\frac{1}{sC_{Z2+}},$$
$$Z_3 = \frac{1}{sC_2} + R_{X+},$$
$$R_3' = R_3 + R_{X-}.$$

where, R_{Y1}, and R_{Y2} are the parasitic resistances and C_{Y1}, and C_{Y2} are the parasitic capacitances at the Y_1 and Y_2 terminals, respectively, R_{Z1+} and R_{Z2+} are the parasitic resistances and C_{Z1+} and C_{Z2+} are the parasitic capacitances at the Z_{1+} and Z_{2+} terminals, respectively, and R_{X+} and R_{X-} represent the parasitic resistances appearing at the X+ and X− terminals, respectively.

5. Simulation Results

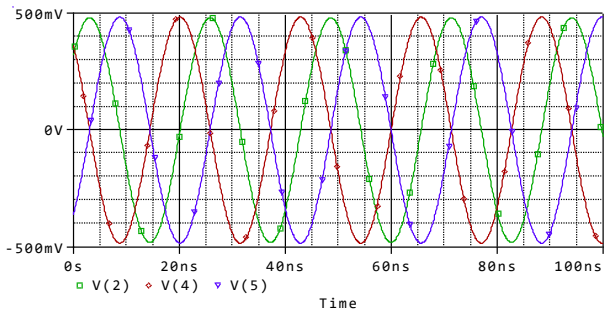
PSPICE simulations of the proposed circuit of quadrature oscillator of Fig. 2 have been performed using the CMOS realization of DV-DXCCII of Fig. 1(b) with 90 nm CMOS parameters as given in Tab. 1. The dimensions of MOS transistors used in DV-DXCCII are given in Tab. 2. The supply voltages and bias voltage are taken as ± 1 V and $V_{BB} = -0.4$ V, respectively. Therefore, the proposed circuit is benifitted with the feature of low operating voltage. The proposed circuit of quadrature oscillator is designed at frequency of oscillation of 39.8 MHz by choosing the passive component values as $C_1 = 1$ pF, $C_2 = 2$ pF, $R_1 = 4$ kΩ, $R_2 = 2$ kΩ and $R_3 = 2$ kΩ. The frequency of oscillation as obtained from simulation is 39.63 MHz which is 0.42 % in error with the designed value. The three voltage outputs and two current outputs along with their Fourier spectrums are shown in Fig. 5 and Fig. 6, respectively. Total Harmonic Distortion (THD) is found to be within 1 %.

Tab. 1: 90 nm CMOS Model parameters.

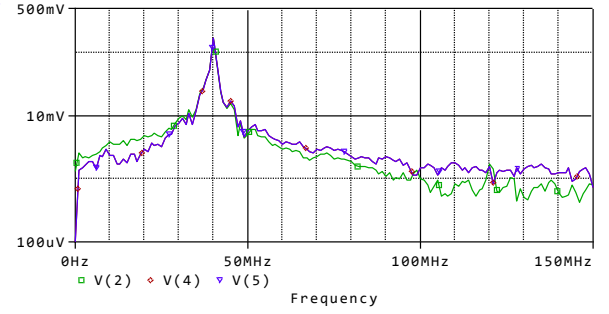
NMOS: LEVEL= 7 BINUNIT= 1 MOBMOD= 2 RDSMOD= 0 CAPMOD= 2 EPSROX= 3.9 TOXE= 2.2E-9 NGATE= 1E20 RSH= 7.2 VTH0= 0.2637059 K1= 0.5459903 K2= -0.106347 K3= 1.00071E-3 K3B= 8.2559564 W0= 1E-10 LPE0= 8.09095E-8 LPEB= 6.541354E-8 DVT0= 0.0241091 DVT1= 0.0354959 DVT= -5.083204E-5 DVTP0= 0 DVTP1= 0 DVT0W=0 DVT1W= 0 DVT2W= -0.032 U0= 180.5863743 UA = 5.007749E-15 UB= 1E-26 UC = -1E-10 EU= 0.1098817 VSAT= 7.526087E5 A0= 2 AGS = 0 B0= 1.248816E-6 B1=1E-7 KETA= 0.05 A1= 0 A2= 1 WINT= 4.513582E-15 LINT=3.004861E-12 DWG= -2.358907E-8 DWB = 4.286229E-8ETA0 = 2.9476E-3 VOFF= -0.0349398 NFACTOR= 1.9128092CDSC= 2.4E-4 CDSCB= 0 CDSCD= 0 ETAB = -0.0117687DSUB= 0.1841044 CIT= 0 PCLM= 0 RDSWMIN= 100PDIBLC2= 0.014020828 PDIBLC1= 0.6278172 PSCBE1=5.552668E8 RSW= 100 PDIBLCB= -1E-3 DROUT= 0.6771686 PVSAT= 1.838993E3 RDWMIN= 0 PSCBE2= 3.09264E-6 PVAG= 0.0491186 DELTA= 1.741612E-3 PRWG= 3 FPROUT= 1.689547E-4 RDSW= 100 RDW= 100 PRWB= 0.0996955 RSWMIN= 0 WR= 1 XPART= 0.5

CGSO= 1E-10 CGBO= 0CF= 0 CGDO= 1E-10 WKETA= 0.039914 PKETA= -1.059394E-3 PETA0= 0 CJS = 8.93E-4 CJD= 8.93E-4 MJS= 0.3003 MJSWGD= 0.1757671 MJD= 0.3003 MJSWS=0.2357 MJSWD= 0.2357 PBSWD= 0.4 CJSWS= 1.59E-10CJSWD= 1.59E-10 CJSWGS= 3.065074E-11 PBSWGS=0.429054 CJSWGD= 3.065074E-11 MJSWGS= 0.1757671PBSWGD= 0.429054 TNOM= 27 PB= 0.4697817 PBSWS= 0.4

PMOS: LEVEL= 7 BINUNIT= 1 MOBMOD= 2 RDSMOD= 0 CAPMOD= 2 EPSROX= 3.9 TOXE= 2.4E-9 NGATE= 1E20RSH= 7.6 VTH0= -0.1828674 K= 0.5378175 K2= -0.100053 K3= 87.186991 K3B= 10 W0= 1.982838E-6 LPE0= 3.624927E-8 LPEB= -1.472555E-8 DVT0= 9.268739E-3 DVT1= 0.050834DVT2= -5.288937E-5 DVTP0= 0 DVTP1= 0 DVT0W= 0DVT1W= 0 DVT2W= -0.032 U0= 100 UA= 2.065422E-15 UB= 1E-23 UC= -1.83813E-17 EU= 1.6379893 VSAT=8.399744E4 A0= 2 AGS= 2.0870724 B0= 1.733997E-7 B1= 1E-7 KETA= 0.05 A1= 0 A2= 1 WINT= 1.540463E-8 LINT=1.382131E-10 DWG= -7.761435E-8 DWB= 2.989342E-8VOFF= -0.0422107 NFACTOR= 3.480545E-3 ETA0= 1E-5ETAB= 0 DSUB= 1 CIT= 0 CDSC= 2.4E-4 CDSCB= 0CDSCD= 0 PCLM= 0.5340493 PDIBLC1= 0.5061971PDIBLC2= 4.729943E-3 PDIBLCB= 0 DROUT= 0.9793851PSCBE1= 1.695917E8 PSCBE2= 3E-6 PVAG= 0.4223462DELTA= 0.0135647 FPROUT= 1.439073E-5 RDSW=872.5912948 RDSWMIN= 100 RDW= 100 RDWMIN= 0RSW= 100 RSWMIN= 0 PRWG= 0.1222031 PRWB= 0.1 WR= 1 XPART= 0.5 CGSO= 1E-10 CGDO= 1E-10 CGBO= 0 CF= 0 CJS= 6.4337E-9 CJD= 6.4337E-9 MJS= 0.475 MJD= 0.475MJSWS= 0.432 MJSWD= 0.432 CJSWS= 1.084E-9CJSWD= 1.084E-9 CJSWGS= 6.3E-11 CJSWGD= 6.3E-11MJSWGS= 0.2169436 MJSWGD= 0.2169436 PB= 0.9646063PBSWS= 0.965 PBSWD= 0.965 PBSWGS= 0.9009362 PBSWGD= 0.9009362 TNOM= 27 WKETA= -0.0364142PETA0= 0 PVSAT= -100



(a)

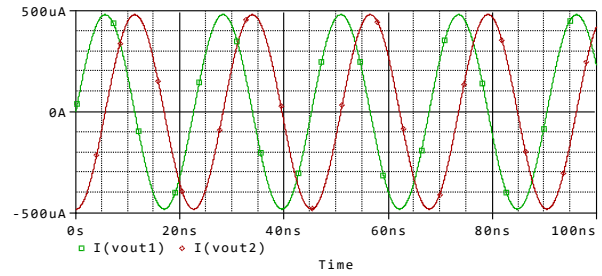


(b)

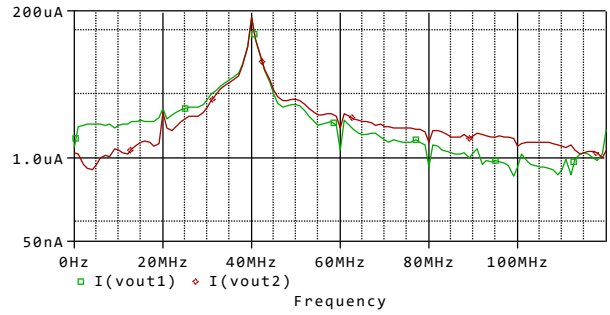
Fig. 5: (a) Three quadrature voltage outputs (b) Fourier spectrum at 39.63 MHz.

Tab. 2: Dimensions of MOS transistors used in DV-DXCCII.

MOS Transistors	W(μm)	L(μm)
M1-M2, M27-M30	0.18	0.09
M3, M7-M8	0.36	0.09
M4-M5	0.3	0.09
M6, M9-M10	0.6	0.09
M11-M20, M31-M34	1.2	0.09
M21-M22	2.61	0.09
M23	5.4	0.09
M24	1.8	0.09
M25	0.72	0.09
M26	0.76	0.09



(a)



(b)

Fig. 6: (a) Two quadrature current outputs (b) Fourier spectrum at 39.63 MHz.

6. Resistorless Load Insensitive, Low Voltage Quadrature Oscillator

In this section, the integration and tuning aspects of the proposed circuit of Fig. 2 have been explored in the form of resistorless realization of load insensitive, low voltage quadrature oscillator. As far as active elements are concerned, its realization in CMOS technology is available. The passive components in form of resistors and capacitors can also be made compatible in CMOS technology [18] and [19]. The resistors can be replaced by active-MOS resistors with added advantage of tunability through external voltage [20]. The resistorless realization of the proposed circuit of load insensitive,

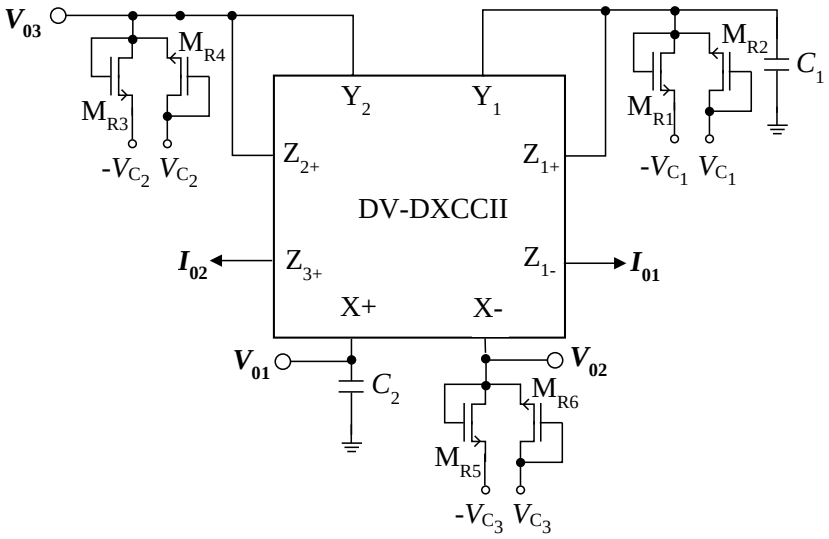


Fig. 7: Proposed resistorless load insensitive, low voltage quadrature oscillator.

low voltage quadrature oscillator is shown in Fig. 7. The resistorless load insensitive, low voltage quadrature oscillator is realized by replacing all the resistors with the two n-MOS transistors based active resistors [20].

The characteristic equation for the resistorless load insensitive, low voltage quadrature oscillator is given as:

$$s^2 + s\left[\frac{1}{C_1 R_{MOS1}} + \frac{1}{C_2 R_{MOS2}} - \frac{1}{C_1 R_{MOS2}}\right] + \\ + \frac{1}{C_1 C_2 R_{MOS1} R_{MOS2}} = 0. \quad (13)$$

The CO and FO are found as:

$$CO: \frac{1}{C_1 R_{MOS1}} + \frac{1}{C_2 R_{MOS2}} \geq \frac{1}{C_1 R_{MOS2}}, \quad (14)$$

$$FO: \omega_0 = \left(\frac{1}{C_1 C_2 R_{MOS1} R_{MOS2}}\right)^{\frac{1}{2}}. \quad (15)$$

All active resistors, R_{MOSk} (where, $k = 1, 2, 3$) is the equivalent resistance of the n-MOS transistors which is defined as:

$$R_{MOSk} = \left[2\mu C_{OX}\left(\frac{W}{L}\right)(V_{Cl} - V_t)\right]^{-1}, \quad (16)$$

where $k,\ l = 1,\ 2,\ 3,$

where, μ, C_{OX}, W/L and V_t are the carrier mobility, gate capacitance per unit area, aspect ratio of n-MOS and threshold voltage.

Next, the resistorless quadrature oscillator is designed for frequency 55 MHz. The transistor aspect ratios for the MOS based active resistors are selected as $(W/L)_{MR1} = (W/L)_{MR2} = (W/L)_{MR3} =$ 7.2 µm/0.09 µm and capacitors values are selected as $C_1 = 1$ pF and $C_2 = 2$ pF. The FO for the proposed resistorless circuit is tuned to 55 MHz by selecting the control voltages $V_{C1} = -V_{C1} = 0.53$ V, $V_{C2} = -V_{C2} = V_{C3} = -V_{C3} = 0.86$ V. The three quadrature voltage outputs and two quadrature current outputs are shown in Fig. 8 and Fig. 9, respectively. The Fourier spectrums of the outputs are shown in Fig. 10 and Fig. 11. The THD is again found to be within 1 %. The obtained results verify the realization of resistorless load insensitive, low voltage quadrature oscillator.

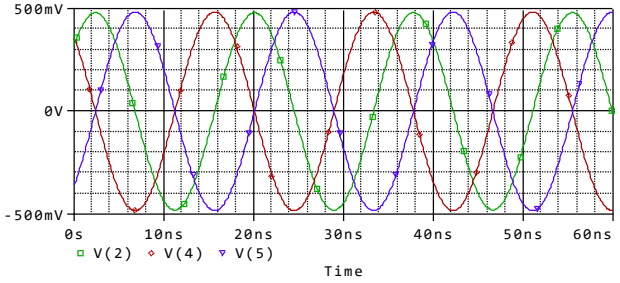


Fig. 8: Three quadrature voltage outputs at 55 MHz.

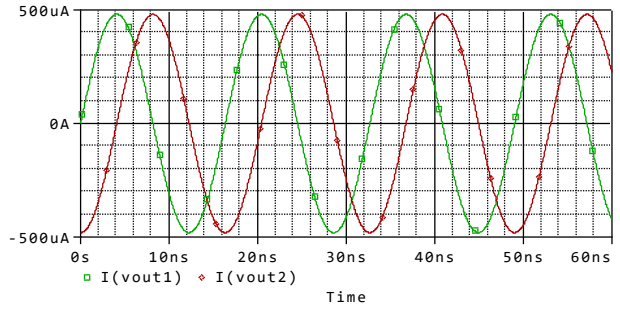


Fig. 9: Two quadrature current outputs at 55 MHz.

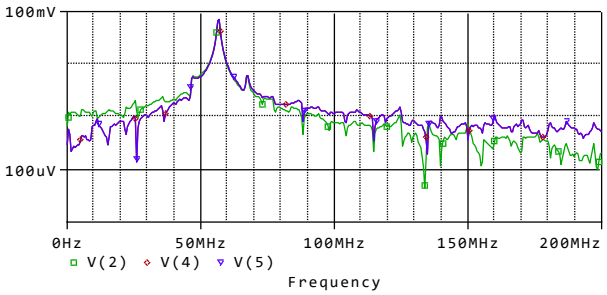


Fig. 10: Fourier spectrums of voltage outputs.

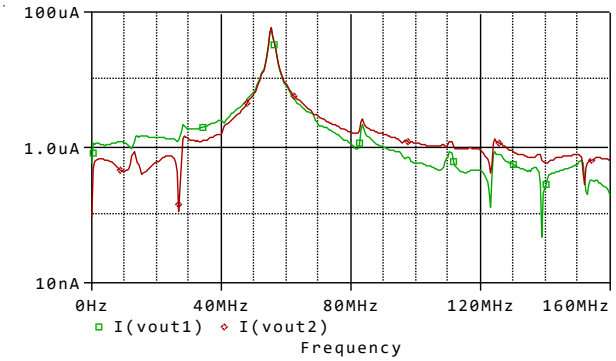


Fig. 11: Fourier spectrums of current outputs.

7. Conclusion

A novel load insensitive, low voltage quadrature oscillator has been presented in this paper. The proposed circuit consists of single DV-DXCCII as active element and all grounded passive components, which is ideal for IC implementation. The proposed circuit of quadrature oscillator provides three quadrature voltage outputs and two quadrature current outputs simultaneously from the same configuration. The proposed quadrature oscillator also offers good active and passive sensitivities. Furthermore, the resistorless realization of the proposed circuit is also explored. Simulations results are given to support the presented theory.

References

[1] WILSON, B. Recent developments in current conveyors and current mode circuits. *IEE Proceedings G (Circuits, Devices and Systems)*. 1990, vol. 137, iss. 2, pp. 61–77. ISSN 0956-3768. DOI: 10.1049/ip-g-2.1990.0014.

[2] ELWAN, H. O. and A. M. SOLIMAN. Novel CMOS differential voltage current conveyor and its applications. *IEE Proceeding Circuits Devices and Systems*. 1997, vol. 144, iss. 3, pp. 195–200. ISSN 1350-2409. DOI: 10.1049/ip-cds:19971081.

[3] SOLIMAN, A. M. Simple sinusoidal RC oscillators using current conveyors. *International Journal of Electronics*. 1975, vol. 42, iss. 4, pp. 309–311. ISSN 0020-7217. DOI: 10.1080/00207217508920504.

[4] AHMED, M. T., I. A. KHAN and N. MINHAJ. On transconductance-C quadrature oscillators. *International Journal of Electronics*. 1997, vol. 83, iss. 2, pp. 201–208. ISSN 0020-7217. DOI: 10.1080/002072197135526.

[5] KHAN, I. A. and S. KHWAJA. An Integrable Gm-C Quadrature Oscillator. *International Journal of Electronics*. 2000, vol. 87, iss. 11, pp. 1353–1357. ISSN 0020-7217. DOI: 10.1080/002072100750000150.

[6] PROMMEE, P. and K. DEJHAN. An Integrable Electronic-Controlled Quadrature Sinusoidal Oscillator Using CMOS Operational Transconductance Amplifier. *International Journal of Electronics*. 2002, vol. 89, iss. 5, pp. 365–379. ISSN 0020-7217. DOI: 10.1080/713810385.

[7] ABUELMAATTI, M. T. and H. A. AL-ZAHER. Current-mode sinusoidal oscillators using single FTFN. *IEEE Transactions on Circuits and Systems-II*. 1999, vol. 46, iss. 1, pp. 69–74. ISSN 1057-7130. DOI: 10.1109/82.749100.

[8] CAM, U., A. TOKER, O. CICEKOGLU and H. KUNTMAN. Current-mode high output impedance sinusoidal oscillator configuration employing single FTFN. *Analog Integrated Circuits and Signal Processing*. 2000, vol. 24, iss. 3, pp. 231–238. ISSN 1573-1979. DOI: 10.1023/A:1008365726144.

[9] ZEKI, A. and A. TOKER. The dual-X current conveyor (DXCCII): a new active device for tunable continuous-time filters. *International Journal of Electronics*. 2002, vol. 89, iss. 12, pp. 913–923. ISSN 0020-7217. DOI: 10.1080/0020721031000120461.

[10] BIOLEK, D., A. U. KESKIN and V. BIOLKOVA. Grounded capacitor current mode single resistance-controlled oscillator using single modified current differencing transconductance amplifier. *IET Circuits, Devices and Systems*. 2010, vol. 4, iss. 6, pp. 496–502. ISSN 1751-8598. DOI: 10.1049/iet-cds.2009.0330.

[11] MAHESHWARI, S. and B. CHATURVEDI. High output impedance CMQO using DVCCs and grounded components. *International Journal of Circuit Theory and Application*. 2011, vol. 39, iss. 4, pp. 427–435. ISSN 1097-007X. DOI: 10.1002/cta.636.

[12] MAHESHWARI, S. and I. A. KHAN. Mixed mode quadrature oscillator using translinear conveyors and grounded components. In: *International Conference on Multimedia Signal Processing and Communication Technologies*. Aligarh: IEEE, 2011, pp. 153–155. ISBN 978-1-4577-1107-7. DOI: 10.1109/MSPCT.2011.6150462.

[13] BEG, P., M. S. ANSARI and M. A. SIDDIQI. DXCC-II based mixed-mode three phase oscillator. In: *International Conference on Multimedia Signal Processing and Communication Technologies*. Aligarh: IEEE, 2011, pp. 9–11. ISBN 978-1-4577-1107-7. DOI: 10.1109/MSPCT.2011.6150507.

[14] BIOLEK, D., A. LAHIRI, W. JAIKLA, M. SIRIPRUCHYANUN and J. BAJER. Realization of electronically tunable voltage-mode/current-mode quadrature sinusoidal oscillator using ZC-CG-CDBA. *Microelectronics Journal*. 2011, vol. 42, iss. 10, pp. 1116–1123. ISSN 0026-2692. DOI: 10.1016/j.mejo.2011.07.004.

[15] MOHAN, J., S. MAHESHWARI and I. A. KHAN. Mixed-mode quadrature oscillators using single FDCCII. *Journal of Active and Passive Electronic Devices*. 2007, vol. 2, iss. 1, pp. 227–234. ISSN 1555-0281.

[16] CHATURVEDI, B. and J. MOHAN. Single DV-DXCCII based voltage controlled first order all-pass filter with inverting and non-inverting responses. *Iranian Journal of Electrical and Electronic Engineering*. 2015, vol. 11, no. 4, pp. 301–309. DOI: 10.22068/IJEEE.11.4.301.

[17] FABRE, A., O. SAAID and H. BARTHELEMY. On the frequency limitations of the circuits based on second generation current conveyors. *Analog Integrated Circuits Signal Processing*. 1995, vol. 7, iss. 2, pp. 113–129. ISSN 1573-1979. DOI: 10.1007/BF01239166.

[18] GEIGER, R. L., P. E. ALLEN and N. R. STRADER. *VLSI Design Techniques for Analog and Digital Circuits*. New York: McGraw-Hill Publishing Company, 1990. ISBN 0070232539.

[19] RAZAVI, B. *Design of analog CMOS integrated circuits*. Boston, MA: McGraw Hill Edition, 2001. ISBN 0072380322.

[20] WANG, Z. 2-MOSFET transresistor with extremely low distortion for output reaching supply voltages. *Electronics Letters*. 1990, vol. 26, iss. 13, pp. 951–952. ISSN 0013-5194. DOI: 10.1049/el:19900620.

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