A Novel Digital Background Calibration Technique for 16 Bit SHA-less Multibit Pipelined ADC

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DOI: 10.15598/aeee.v14i5.1592

Abstract. *In this paper, a high resolution of 16 bit and high speed of 125 MS·s^{-1}, multibit Pipelined ADC with digital background calibration is presented. In order to achieve low power, SHA-less front end is used with multibit stages. The first and second stages are used here as a 3.5 bit and the stages from third to seventh are of 2.5 bit and last stage is of 3-bit flash ADC. After bit alignment and truncation of total 19 bits, 16 bits are used as final digital output. To remove linear gain error of the residue amplifier and capacitor mismatching error, a digital background calibration technique is used, which is a combination of Signal Dependent Dithering (SDD) and butterfly shuffler. To improve settling time of residue amplifier, a special circuit of voltage separation is used. With the proposed digital background calibration technique, the Spurious-Free Dynamic Range (SFDR) has been improved to 97.74 dB @ 30 MHz and 88.9 dB @ 150 MHz, and the signal-to-noise and distortion ratio (SNDR) has been improved to 79.77 dB @ 30 MHz, and 73.5 dB @ 150 MHz. The implementation of the Pipelined ADC has been completed with technology parameters of 0.18 µm CMOS process with 1.8 V supply. Total power consumption is 300 mW by the proposed ADC.*

Keywords

Butterfly, CMOS, digital background calibration, op-amp, pipelined ADC, SHA-less front-end, Signal Dependent Dithering.

1. Introduction

Various digital applications, such as communication base stations, cable head end, professional HDTV cameras and video digitizers require Analog to Digital Converters (ADCs) of high-resolution, high-speed and low cost [1], [2] and [3]. Moreover, the modern IF-sampling super heterodyne communication systems require an DC of reduced receiver complexity, reduced overall system cost and should be able to sample input signals above 150 MHz. It's a big challenge for designers to implement a low power Pipelined ADC of high sampling rates with more than 16-bit resolution, which could be good for high speed data communication. Different types of errors like op-amp nonlinearity, capacitor mismatch and finite op-amp gain may come in MDAC, which degrades the performance and limit the resolution of Pipelined ADC. Linear errors like finite op-amp gain and capacitor mismatch could be removed by using various techniques [4], but to minimize nonlinear errors, very few techniques are available in the industry [5]. Many digital background calibration techniques have been developed due to limitations of analog circuits. Moreover, CMOS is the technology which is preferably used to implement switched capacitor circuits due to its low cost. Similar types of pipelined ADCs are the most popular in mobile communication systems.

A low power 16-bit, 125 MS·s^{-1} pipelined ADC is presented here for high resolution applications. To save power, the dedicated front-end Sample and Hold Amplifier (SHA) has been removed, which also permits ADC to use a smaller input sampling capacitor to facilitate its drivability. But the SHA-less architecture causes some problems like IF sampling front-end, which could be removed by using specific circuit designs [6]. By using a multi-bit front-end stage, additional power

could be saved, but the circuit complexity will increase. The proposed Pipelined ADC adopts a multi-bit structure, where the first and second stages are of 3.5 bit, whereas other stages from 3 to 7 are of 2.5 bit each, and the 3-bit Flash ADC works as the last stage. To minimize the effects of nonlinear gain errors, a two-stage amplifier with a gain-boosted structure is implemented in the first stage to realize a high swing and high gain op-amp. The capacitor mismatches and linear gain errors are corrected by a combination of techniques, named as Signal Dependent Dithering (SDD) [7] and Butterfly Shuffler (BS) [8]. These techniques are useful for removing small signal linearity errors. Due to capacitor mismatching and other non-idealities of Op-amp, the ADC transfer function may be affected by discontinuities produced by DNL errors. By using dithering, the problem gets resolved as described in this paper. By using CMOS process technology, performance requirement gets reduced and simplifies the design of the analog circuit by inserting a digital algorithm. The calibration algorithm requires an extra circuit between sub-ADC and sub-DAC, which introduces the problem of an extra delay as well as reduces the settling time for residue amplifier. To remove these problem, a properly adjusted clock is used, which could control the switch to short differential outputs of Op-amp in hold phase. To remove the interference between different stages, separate voltage references are used. So, the first two stages are using different voltage reference than the other backend stages of Pipelined ADC. It has large transient current to charge and discharge capacitors in hold phase to backend stages, which is another reason to use different voltage references here.

Different sections of this paper is as follows. In Section 2. , front-end considerations are discussed. In Section 3. , the implementation details of the major circuit blocks of the proposed pipelined ADC are discussed. Both the dithering and butterfly calibration techniques used for the proposed pipelined ADC are discussed in Section 4. Section 5. presents the measurement results for the proposed ADC. The summary & conclusion of this paper is the part of Section 6.

2. Front-End Considerations

It was a dream to accomplish high SNDR and low power dissipation simultaneously in early Pipelined ADC designs. To achieve high SNDR, it requires a large sampling capacitors, which increases power dissipation along with circuit complexity. By using the advantages of bipolar devices, BiCMOS technology could solve the problem of drivability of Pipelined ADC [9]. And, by using CMOS technology, the problem of large input sampling capacitor could be resolved by the switched-capacitor CMOS pipelined ADCs where on-chip input buffer has been removed. In pipelined ADC, a dedicated front-end SHA is most commonly used, which highly contributes to noise, distortion and consume significant power for the complete Pipelined ADC unit. So, by removing SHA, power dissipation can be reduced along with noise reduction. Also, reducing the number of those stages which contribute to noise is the best solution to increase SNDR and SFDR without using large sampling capacitors.

In this way, other stages of Pipelined ADC can work well even with smaller sampling capacitors to minimize the overall circuit's noise and power. By using the smaller values of the input sampling capacitors, the sizes of switches can be reduced further to attain the same bandwidth, and hence the nonlinear parasitic capacitance in the input sampling network could be reduced [10]. Further the linearity of sampling circuit has improved, but the complexity of circuit gets increased with the multi bit ADC architecture [11] and [12].

A single stage amplifier has been considered here with an effective trans-conductance (gm) and feedback factor (β), whose results are also applicable to a two-stage amplifier. So, the Bandwidth (BW) for that is given by the Eq. (1):

$$BW = \beta \frac{gm}{CL}. \tag{1}$$

By adding each bit in stage-1, feedback factor β becomes halved, so the load capacitor *(CL)*, goes half to keep bandwidth constant, whereas power dissipation remains constant. Here, the load capacitor *(CL)* is actually the addition of the effective loading caused by the feedback capacitor *(Cf)*, sampling capacitors *(Cs)* of stage-1, the overall sampling capacitance of stage-2 *(Cs2)* and parasitic capacitances. If CL has been dominated by *Cs2* then CL can be halved by making half of *Cs2* to make BW constant. There are two major sources of noise, which contributes to the accumulative noise sampled by stage-2 ($\sigma 2$) and the first source of the noise in the stage-2 sampling circuit is due to the switches ($\sigma 2\_ST$). When the stage-1 amplifier is in hold phase, the noise occurred that time acts as another major source of noise ($\sigma 2\_AP1$). By referring to the input of the ADC, $\sigma 2\_ST$ can be written as Eq. (2):

$$\sigma 2\_ST \alpha \sqrt{\frac{KT}{CL}}/G. \tag{2}$$

So, there is a reduction factor of $\sqrt{2}$ by which $\sigma 2\_ST$ has been reduced. Equation (3) and Eq. (4) represent $\sigma 1$ and $\sigma 2\_AP1$ respectively, which stay moderately unaffected to first order when referred to input and stage-1 samples the track mode noise. *Cp* indicates

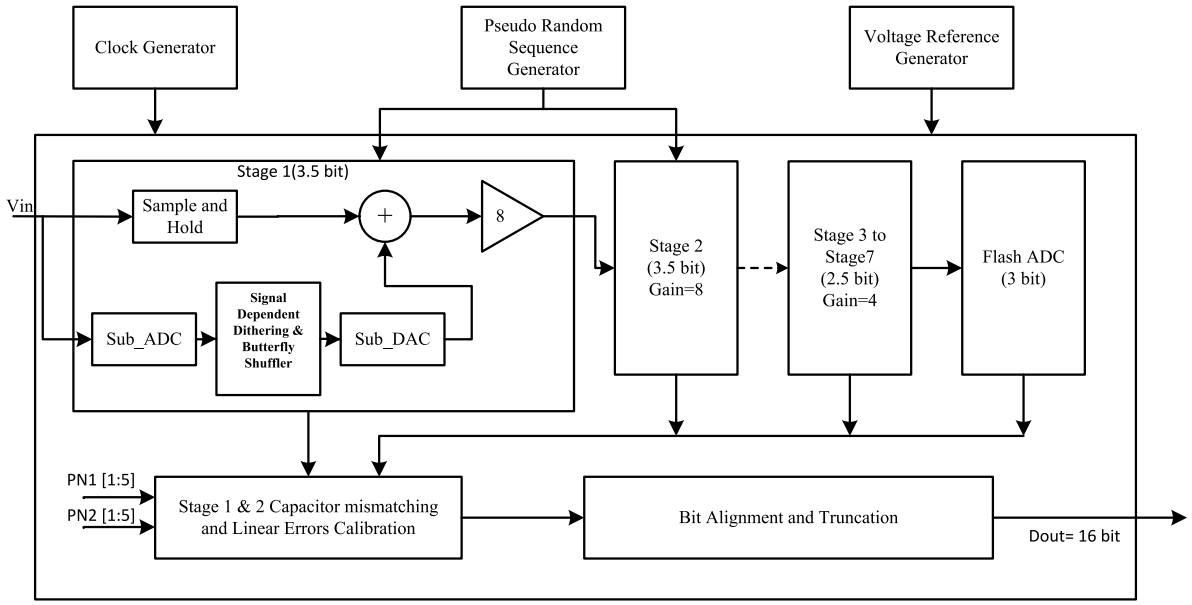

Fig. 1: Proposed 16 bit SHA-less multi-bit Pipelined ADC.

the summing node parasitic capacitance of stage 1.

$$\sigma 1 \alpha \sqrt{\frac{KT(Cs + Cf + Cp)}{Cs^2}} = \sqrt{\frac{KT}{\beta GCL}}, \quad (3)$$

$$\sigma 2\_AP1 \alpha \sqrt{\frac{KT}{\beta CL}}/G. \quad (4)$$

It's indicated from the equations above that by adding each quantized bit in the first stage, the gain will increase by two, at the same time some other factor will decrease by two, which is the feedback factor. So, there is the requirement to make a balance between power and number of bits. Here, SHA-less front-end has been chosen to achieve low power, high SNDR, high SFDR and minimum value of sampling capacitors but at the price of circuit complexity particularly for sampling frequencies near 200 MHz.

3. Proposed Pipelined ADC

In Fig. 1, the block diagram of 16-bit pipelined ADC is shown. The first two stages of the 16-bit Pipelined ADC are of 3.5 bits, the succeeding seven stages are of 2.5 bits each, and the 3-bit flash ADC has chosen for the last stage. To get a solution for high resolution of 16 bits, for low power consumption and for removing the capacitor mismatching problem, the first stage used here is of 3.5 bits. Multi-bit Pipelined ADC is much better than the Pipelined ADC, having all stages of the same kind. Sometimes, these multi-bit Pipelined ADCs are used even without calibration because these are able to save more power [22]. A problem that may arise here is the complicated MDAC circuit designing, when resolution becomes higher than 4 bit. So, whereas the initial stages are of higher resolution, the succeeding stages have comparatively low resolution. As the number of stages are going to be scaled down along the pipelined ADC chain, the problem of capacitor mismatching and higher bias currents will be relaxed. Less area utilization is the additional benefit of multibit structured ADC because most of the stages are of low bit size.

The proposed architecture consists of a reference generator, pseudo random sequence generator, digital calibration block, bit alignment and truncation block, different stages of ADC of different bit size and clock generator. A voltage reference generator is used with low temperature coefficient and high Power Supply Rejection Ratio (PSRR). The clock generator is able to generate low jitter clocks for high input sampling frequencies. The capacitor mismatching and the residue amplifier's linear gain errors are corrected by digital background calibration which combines two techniques as SDD and butterfly shuffler. Two pseudo random noise sequences PN1 [1:5] and PN2 [1:5] are used to control Signal Dependent Dithering (SDD) and butterfly shuffler. The final 16-bit digital output can be achieved through digital bit alignment and truncation method.

3.1. SHA-Less Front-End

As SHA-less front-end has been used in this Pipelined ADC, both the multiplying DAC (MDAC) and the flash concurrently are able to sample the input signal.

The flash produces quantized output, which initiates MDAC to generate the residue signal for the next stage. The value of gain has been set to 8 for the MDAC of stage-1, and gain value set to 4 for stage 3 to stage 7. The stage-1 is able to quantize 4 bits and one bit out of those is a redundant bit, which is used to tolerate comparator offsets [15].

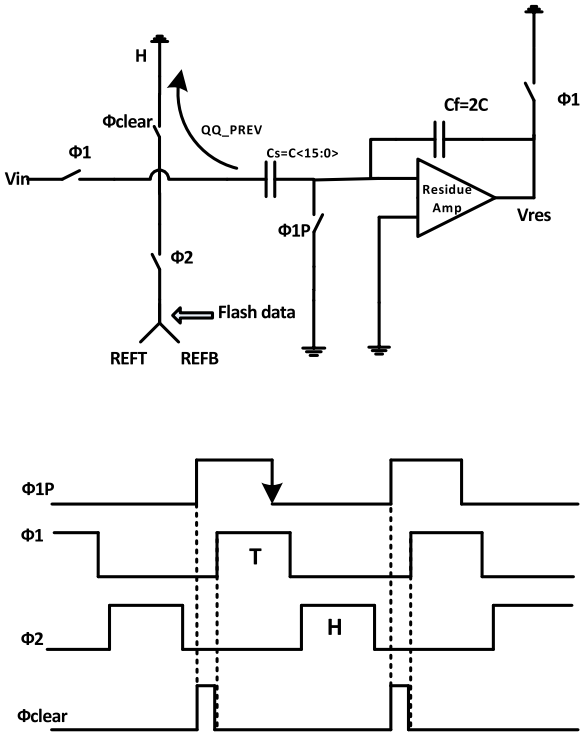

Fig. 2: Removing the nonlinear charge kickback to Vin, 4-bit stage-1 MDAC operation with Φ clear.

Figure 2 shows the stage-1 as a 4 bit MDAC with Φclear to eliminate the nonlinear charge kickback to Vin. The non-linear kickback could be settled, but the fact of how fast depends the value of Cs and sampling rate [14]. Another factor of the circuit which can be taken care of is effective impedance, as it drives the input. So, a large value of Cs is required for low noise coupled to stage-1 with its input buffer. This will avoid the kickback. The sampling flash architecture is used for the SHA-less front end to reduce the mismatch effects between the flash and the signal sampled by the MDAC [16] and [17].

Figure 3 shows the SHA-less stage-1 Switched-capacitor implementation of 4-bit without any dithering [22]. During the track phase Φ1, the flash sampling capacitors (C1s_fl) and the sampling capacitor (Cs) are concurrently sampling Vin. Also, sampling the reference ladder is completed by a different set of capacitors in the flash (C1ref_fl). To keep track of the input signal and to minimize sampling distortion, linear bootstrapped input switches are used to perform this task [18] and [19]. C1s_fl and C1ref_fl are short together at the beginning of Φ2, to produce input for the pre-amplifier, and latch to produce valid flash data together with a small delay. The flash data is used to produce the residue voltage (Vres) which is driven by the MDAC reference switches used at the output of the residue amplifier. Here, during Φ2, the most challenging job is to achieve the total delay over the pre-amplifier and the latch, for the available settling time for MDAC. So, both the residue amplifier and flash comparators have to be faster in this SHA-less front-end, which consumes more power in SHA-less front-end as compared to a conventional one.

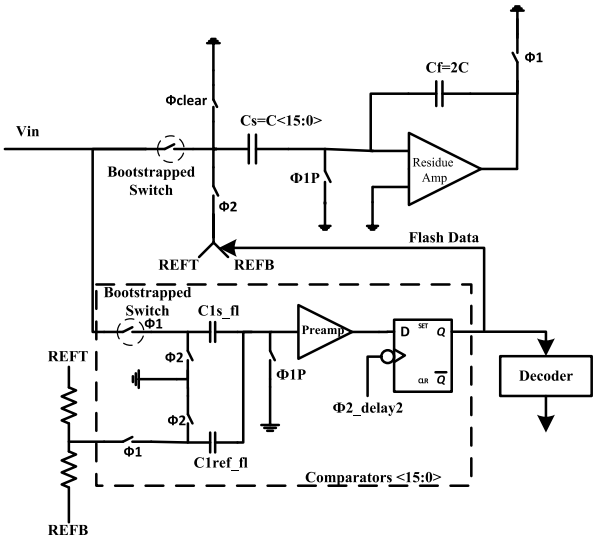

Fig. 3: SHA-less Stage-1, 4 bit Switched-capacitor implementation.

The choice between SHA-less front-end and conventional SHA front-end depends upon the application because by eliminating the SHA, power could be saved but for medium resolution and medium sampling rates only. For high resolution and very high sampling rate, power saving is difficult as flash comparators could use the maximum time offered for MDAC settling. So, the designing of fast and low-power comparators is practically a challenging job. Even for high sampling rates ADCs, SHAs are designed specifically for the application, which cannot be generalized. Here a precise design of SHA-less architecture with high sampling rate of 125 MS·s^{-1} is presented, which is capable to save power significantly. Since Cs and C1s_fl are simultaneously sample Vin, a problem that may arise in SHA-less front end is the difference between the values of flash and values sampled by the MDAC. It may use the available correction range, and sometimes it causes different sampled values than actual, due to timing and bandwidth mismatch between MDAC sampling networks and the flash ADC. Also for higher input frequencies, the difference becomes high and if frequencies increase further, stage-1 may cross the range of correc-

tion, which may result in missing codes. Hence, the important factor is to reduce the sampling mismatch and to increase the range of tolerance so that it always comes within the correction range. To get a complete range of codes, without any missing one, it should fulfil the following equation:

$$|\text{Sampling mismatch} + \text{Flash offsets}| < \text{VREF}/2^4. \quad (5)$$

To maximize the tolerance of sampling mismatch, their offsets should be minimized and offset cancellation could be used [20]. So, the fast comparators, used here for stage-1, are subject to offsets with high values to satisfy offset cancellation requirement. Due to the sampling flash architecture for the sampling capacitor (C1s_fl) and the reference capacitor (C1ref_fl), the capacitive reduction of 2 can be achieved in advance for pre-amplification, which doubles the flash offset and refers to input as associated to normal flash. In the stage-1, with increase in number of bits, the tolerance of sampling mismatch would double the available correction range and the design would be easy. The comparators are relaxed now from offset cancellation problem as matching requirement between MDAC sampling network and flash has been resolved but at the cost of high power consumption. To drive the sampling switches to minimize the timing skew concerning the MDAC sampling and flash clocks, the same buffered clock edge has been used here.

Since the two networks are different, matching their bandwidths is a tricky job as Cs is much larger than C1s_fl. The second reason is that the flash network is made up of two equal capacitors (C1s_fl and C1ref_fl), whereas the MDAC has two unequal capacitors, a large Cs and a small Cf. The third reason is that the parasitic capacitance of pre-amplifier is much lower than the residue amplifier. In-spite of all the differences, the bandwidths could be matched for two networks using post layout extracted simulations. The circuits could be cautiously by taking care of bandwidth, comparator offset cancellation and timing matching. SHA-less ADC can be sample inputs beyond 300 MHz and within the correction range itself.

3.2. Flash Comparator

The flash comparator for stage-1 is similar to [17] but without cross-coupled PMOS pairs with the advantage of shorter regeneration time as shown in Fig. 4. In this comparator, PMOS are used as loads to make up a pre-amplifier. Here a diode is coupled to a latch and PMOS loads. When Φ2 begins, the pre-amplifier starts to amplify the input signal up to the peaks of different nodes.

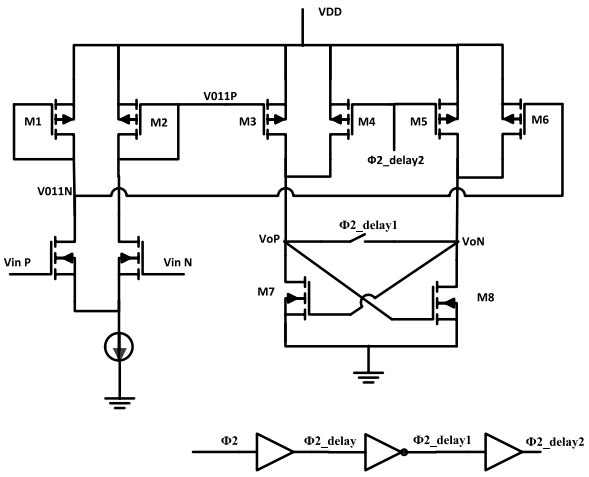

Fig. 4: Flash comparator circuit for Stage-1.

3.3. Residue Amplifier (RA)

The residue amplifier used here is basically a Two-stage Miller-compensated design as shown in Fig. 5, and it is able to give high gain, large swing and excellent linearity [21] and [22]. The telescopic structure with PMOS inputs are used here for the first stage and NMOS differential pair with PMOS loads are used at the second stage. There is a large gm per unit current, so NMOS inputs should be in the first stage of the Residue Amplifier. But for CMOS process technology, there is an indication of greater value of 1/f noise, if NMOS devices are used comparatively to PMOS devices. A problem of low frequency nature of 1/f noise could be solved

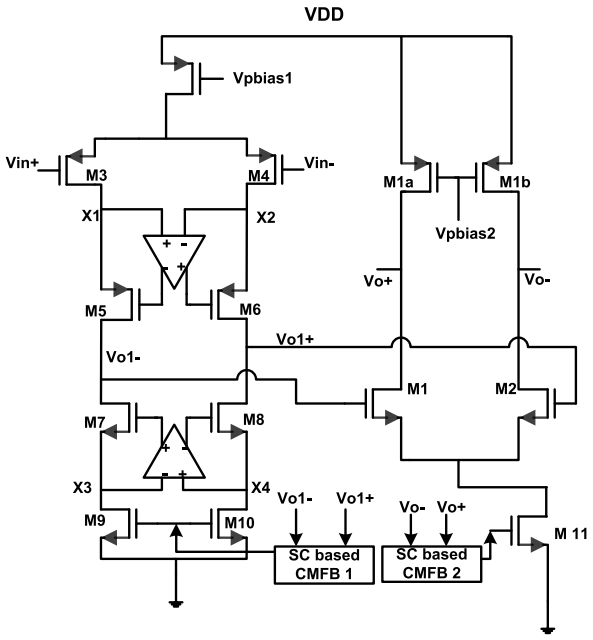

Fig. 5: Residue Amplifier circuit for Stage-1.

by growing the Miller capacitor, which can directly filter the noise. Therefore, a large Miller capacitor is used here. On the other side, an auto-zeroing amplifier could be used, which would help to reduce 1/f noise but at the price of increased circuit complexity and power consumption. To get the lowest power solution, PMOS inputs are preferably used for stage-1 due to their lower 1/f noise nature.

3.4. Voltage References

To supply stable voltages to all stages of Pipelined ADC, specific Voltage reference structure is used as mentioned by Keetal, [27]. Using this voltage referencing arrangement, there will be no effect on final digital output because digital calibration performed for the first two stages will be passed to backend stages as well. When hold phase comes, depending upon outputs of sub_ADC, the sampling capacitor may charge or discharge with sub_DAC's reference voltages. If just one reference voltage was used, a large current would be required by the capacitors of the first stage, and the transient output of other stages may lead to slow settling, hence two different voltages are used here. When the hold phase starts, the sampling capacitors also start, which supplies small current. By using separate voltages, the final outputs will be unaffected. In this way, the current utilization would be optimized and hence power could be saved.

4. Proposed Calibration Technique

High gain Op-amps are used here in this design at each stage to remove nonlinear errors and capacitor mismatching. The linear gain errors are treated together and could be corrected by the background digital calibration technique. For this design, Signal Depended Dithering (SDD) [7] is used with butterfly Shuffler [8]. For a 3.5 bit MDAC stage, the transfer function is changed for SDD with fifteen additional comparators al a15 as shown in Fig. 6.

Depending on the current PN code and the location of output residue voltage (*Vres*), dithering is injected here. For the calibration algorithm of 3.5 bit MDAC stage, the circuit modifications has to be done as per the residue plot's requirements, indicated clearly in Fig. 6.

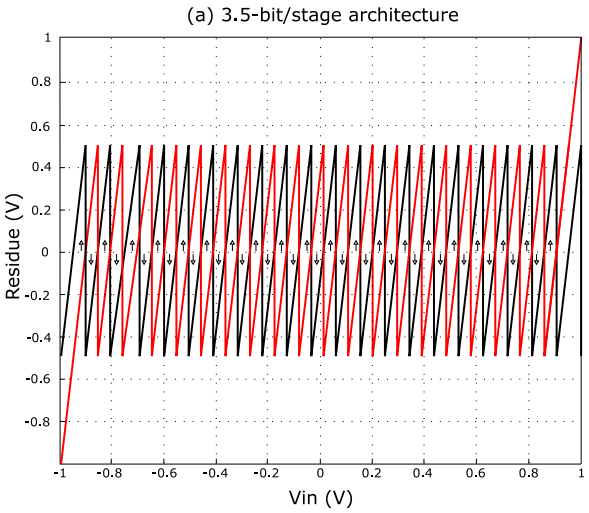

Fig. 6: Determination of Signal Dependent Dithering in Residue plot for a 3.5 bit MDAC stage.

For PN [2:5] =4'b0000, the transfer function can be expressed as per following equation:

$$\begin{aligned} Vres &= G \cdot \left[Vin - \sum_{i=1}^{14} \left(Di \cdot Vref \frac{Ci}{Cs} \right), \right. \\ &\quad \left. -PNdither \cdot Vref \cdot \frac{C15}{Cs} \right], \\ \text{where } G &= \frac{Cs}{Cf + (Cs + Cf + Cp)/A}, \\ \text{and } Cs &= \sum_{i=1}^{16} Ci. \end{aligned} \tag{6}$$

The equivalent sampling capacitor is *Cs*, the feedback capacitor is *Cf*, the equivalent input parasitic capacitor of op-amp is *Cp* and the actual gain of the residue amplifier is G. When PN [2:5] is equal to 4'b0000, the dithering signal is injected to C15 and D1 D14 are the fourteen normal outputs of sub_ADC. PNdither is equal to (PN [1] +loc_res) 2, where PN sequences PN [1] = -1, 1 and loc_res decides the location of output residue Vres. If Vres is on the upper half plane of residue graph Fig. 7, loc_res=1 makes PNdither = 0, 1 which means the transfer curve can move down or remains unchanged. The transfer curve can move up or remains unchanged, when loc_res= -1, which makes PNdither = 0, -1. To extract the errors, Eq. (6) multiplies by -2 so,

$$
\begin{aligned}
Vres(-2)\cdot PN[1] &= -2G\left[Vin-\sum_{i=1}^{14}\left(Di\cdot Vref\frac{Ci}{Cs}\right)\right.\\
\left(\frac{PN[1]+loc_res}{2}\right) &\cdot Vref\cdot\left.\frac{C15}{Cs}\right]PN[1]\\
&= PN\_modulate + G\cdot Vref\cdot\frac{C15}{Cs}\\
&as\ PN[1]^2=1\\
\text{where } PN\_modulate &= -2G\left[Vin-\sum_{i=1}^{14}\right.\\
\left(Di\cdot Vref\frac{Ci}{Cs}\right) &-\left(\frac{loc\_res}{2}\right)Vref\cdot\left.\frac{C15}{Cs}\right]\cdot PN[1].
\end{aligned}
\tag{7}
$$

As loc_res is not related to PN [1] so, PN_modulate can be assumed as a noise that could be avoided with the help of a low-pass filter, which is ideally an accumulator and is able to average a large quantity of samples. So, the Eq. (8) is another way to write the Eq. (7):

$$
\begin{aligned}
WG,15 &= \frac{1}{N}\sum_{i=1}^{N}-2Vres(n)\cdot PN[1]|N\to\infty\\
&= G\cdot Vref\cdot\frac{C15}{Cs}.
\end{aligned}
\tag{8}
$$

By considering infinite samples, whose average has been taken, WG,15 would include both capacitor mismatches and linear gain error. By using Butterfly Sampling technique for injecting dithering to each capacitor Ci (i= 1 to 16), which is controlled by four bit PN sequence PN [2:5] shown in Fig. 7. Total of 16 different WG (i=1 to 16) are obtained from Eq. (8) and saved to their respective registers, which are marked as WG,i (i=1 to 16) is shown in Tab. 1.

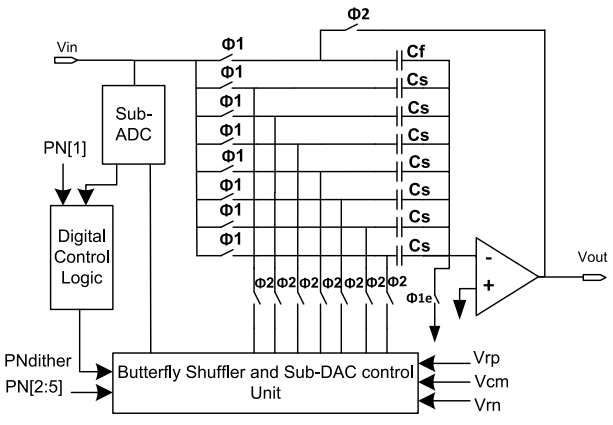

Fig. 7: 3.5 bit MDAC stage's circuit modifications for calibration.

The working of butterfly shuffler is illustrated in Fig. 8. The final digital output after calibration and by assuming backend stages are ideal, will be equal to G.Vin/4 which is linear.

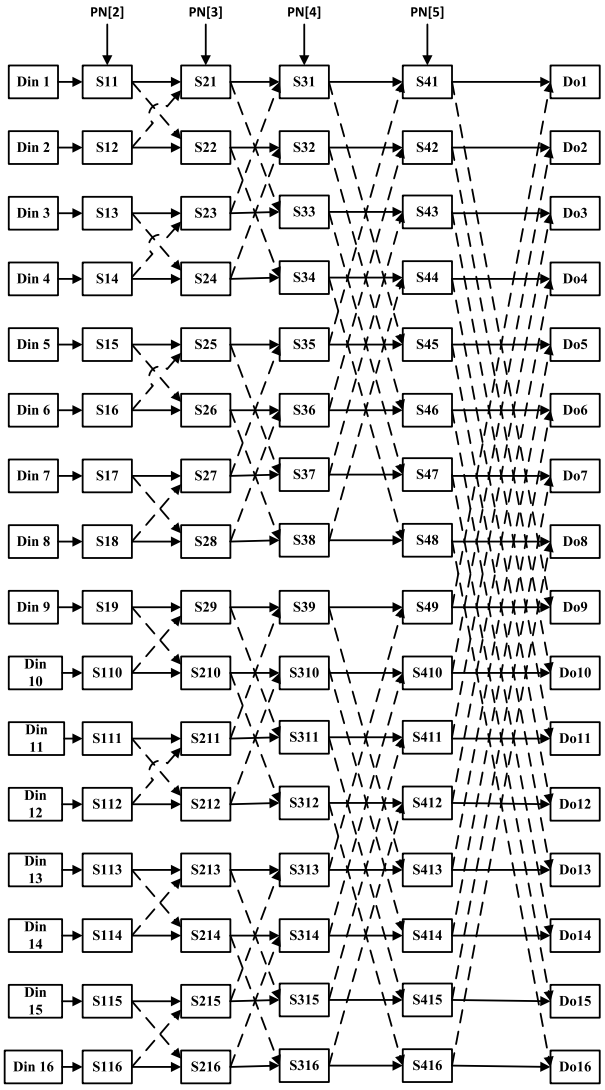

Fig. 8: Butterfly shuffler for 3.5-bit stage.

5. Results and Measurements

A two-stage Miller compensated Op-amp topology has been used for the proposed 16-bit Pipelined ADC to attain a large output swing and a high gain. As in this design, the first stage requires a larger gm and a higher gain, so the first stage of Op-amp uses NMOS inputs with a telescopic and gain-boosting structure. With design margins and process variations, the first two stage's loop gains are slightly different to each other.

Figure 9 shows the SNDR and SFDR response of the ADC for w.r.t to input frequency range of 30 MHz to 150 MHz at sampling frequency at 125 MS·s^{-1}. With the increase in frequency SFDR decreases due to increase in parasitic capacitance and decrease in gain. Figure 10 shows the values obtained by applying the FFT at 125 MS·s^{-1} without calibration, and the values of SFDR and SNDR are 80 dB and 70.28 dB respectively. Five different frequencies ranging from 30 MHz

Tab. 1: Total of 16 different WG (i=1 to 16) has saved to the respective registers.

PN [2:5]	Do 1	Do 2	Do 3	Do 4	Do 5	Do 6	Do 7	Do 8	Do 9	Do 10	Do 11	Do 12	Do 13	Do 14	Do 15	Do 16
0000	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	*	0
0001	D9	D10	D11	D12	D13	D14	*	0	D1	D2	D3	D4	D5	D6	D7	D8
0010	D5	D6	D7	D8	D1	D2	D3	D4	D13	D14	*	0	D9	D10	D11	D12
0011	D13	D14	*	0	D9	D10	D11	D12	D5	D6	D7	D8	D1	D2	D3	D4
0100	D3	D4	D1	D2	D7	D8	D5	D6	D11	D12	D9	D10	*	0	D13	D14
0101	D11	D12	D9	D10	*	0	D13	D14	D3	D4	D1	D2	D7	D8	D5	D6
0110	D7	D8	D5	D6	D3	D4	D1	D2	*	0	D13	D14	D11	D12	D9	D10
0111	*	0	D13	D14	D11	D12	D9	D10	D7	D8	D5	D6	D3	D4	D1	D2
1000	D2	D1	D4	D3	D6	D5	D8	D7	D10	D9	D12	D11	D14	D13	0	*
1001	D10	D9	D12	D11	D14	D13	0	*	D2	D1	D4	D3	D6	D5	D8	D7
1010	D6	D5	D8	D7	D2	D1	D4	D3	D13	D13	0	*	D10	D9	D12	D11
1011	D14	D13	0	*	D10	D9	D12	D11	D6	D5	D8	D7	D2	D1	D4	D3
1100	D4	D3	D2	D1	D8	D7	D6	D5	D12	D11	D10	D9	0	*	D14	D13
1101	D12	D11	D10	D9	0	*	D17	D13	D4	D3	D2	D1	D8	D7	D6	D5
1110	D8	D7	D6	D5	D4	D3	D2	D1	0	*	D14	D13	D12	D11	D10	D9
1111	0	*	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1

*Pndither

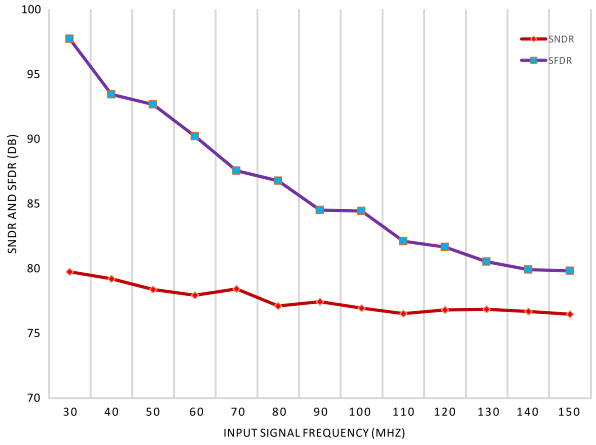

Fig. 9: Measured SFDR and SNDR at versus input signal frequency.

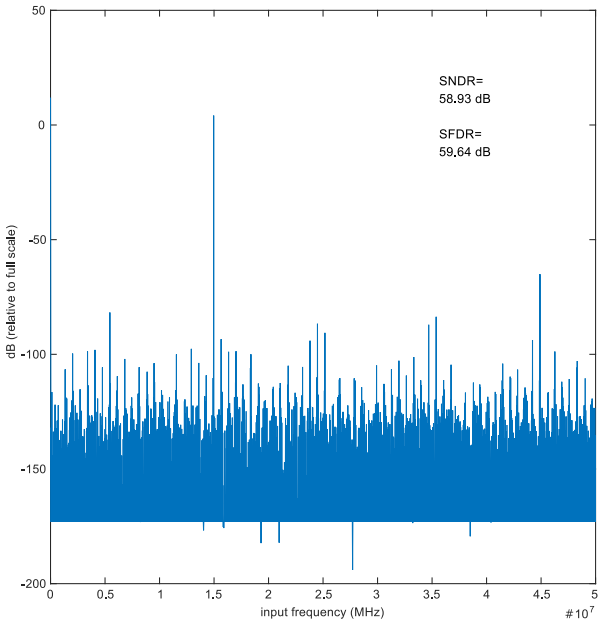

Fig. 10: Measured FFT before calibration.

to 150 MHz are given to the ADC to test its dynamic performance, which indicates that the SNDR and SFDR give better results for input signal below 150 MHz. Figure 11 shows the values of the SFDR and SNDR obtained by applying the FFT of sampling a 30 MHz full-scale input at 125 MS·s^{-1}, and is able to achieve SFDR and SNDR of 97.74 dB and 79.77 dB, respectively. Figure 12 shows the values of SNDR and SFDR after applying an FFT of sampling a 150 MHz input, and achieves an SFDR and SNDR of 88.9 dB and 73.5 dB respectively. Based on different results, ADC has been tested after subtracting out the jitter of the clock generator used. As per SNR measurements, the estimation of internal jitter of the ADC is 70 fs. The indication of low-jitter in the clock circuit is the slow drop of SNDR at high frequencies.

The DNL is improved from +1/-1 to 0.57/-0.48 and INL has improved from 8.7/-8.8 to 0.5/-0.5 after calibration as shown in Fig. 13 and Fig. 14. The total power consumption of the proposed ADC is 300 mW, which includes the CMOS output drivers, operating at a 1.8 V supply. The calibration time for stage 1 and 2 is about 40s with sampling rate as 125 MS·s^{-1}. The performance comparison of proposed ADC, with other Pipelined ADCs [21], [22], [23], [24], [25] and [26] are presented in Tab. 2.

The ADC of [21] is a 14-bit Pipelined ADC, implemented in Nano technology of 90 nm, but due to high values of INL and DNL, it has limited scope. Because all digital post processing has been done off-chip with help of a PC, which hasn't integrated on a chip considered as another problem of this ADC. The ADC in [22] is a 16-bit 125 MS·s^{-1} SHA-less 4-bit front-end, which is able to achieve high values of SFDR and

Tab. 2: Comparison Table.

Parameter	[21]	[22]	[23]	[24]	[25]	[26]	This work
Technology (µm)	0.09	0.18	0.18	0.25BiCmos	0.18	0.18	0.18
Resolution	14	16	14	16	14	10	16
Sampling Rate	100 MS·s^{-1}	125 MS·s^{-1}	60 MS·s^{-1}	160 MS·s^{-1}	100 MS·s^{-1}	165 MS·s^{-1}	125 MS·s^{-1}
Supply (V)	1.2	2	1.6	3.3/5	1.8	1.8	1.8
INL (LSB)	1.3	1.5	0.6	4	3.86	0.6	0.57
DNL (LSB)	0.9	0.5	0.5	1.6	0.65	0.41	0.5
SNDR (dB)	73	78.6	73.3	76.16	69.1	56.1	79.77
SFDR (dB)	90	87	84	102	82.7	64	97.74
Power (mW)	250	385	67.8	1600	121	22	300

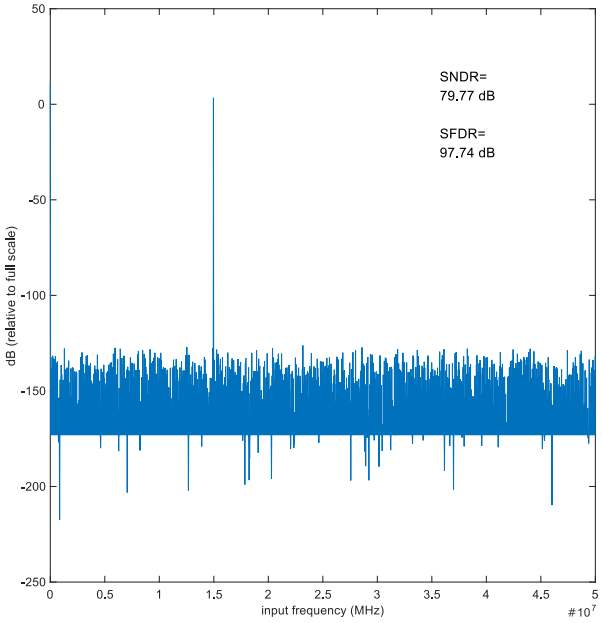

Fig. 11: Measured FFT when ADC is sampling a 30 MHz input at 125 MS·s^{-1}.

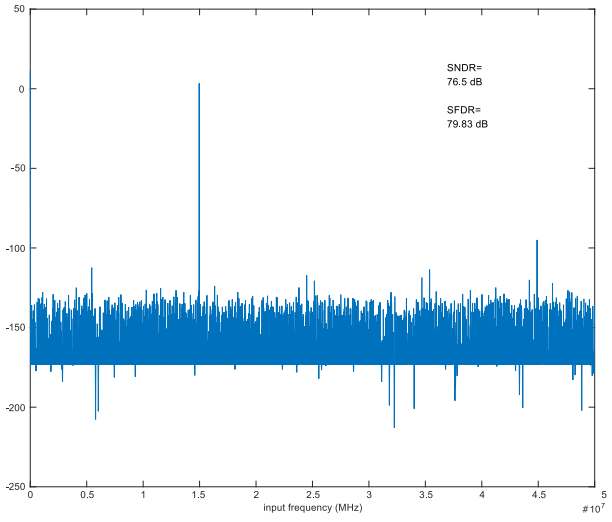

Fig. 12: Measured FFT when ADC is sampling a 150 MHz input at 125 MS·s^{-1}.

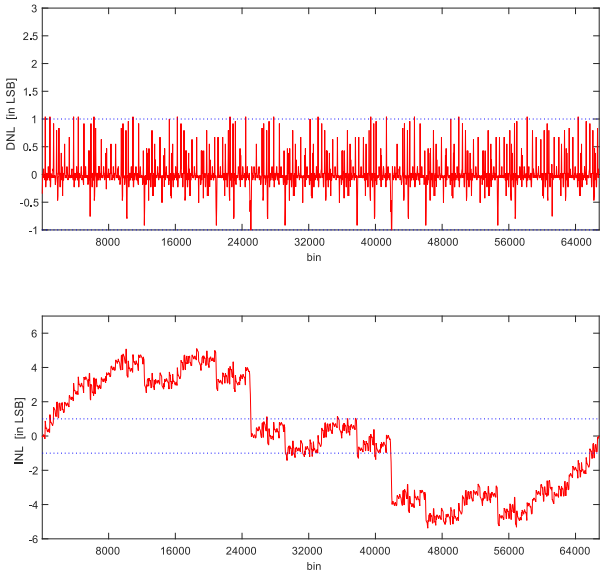

Fig. 13: Measured DNL and INL of ADC at 125 MS·s^{-1} before Calibration.

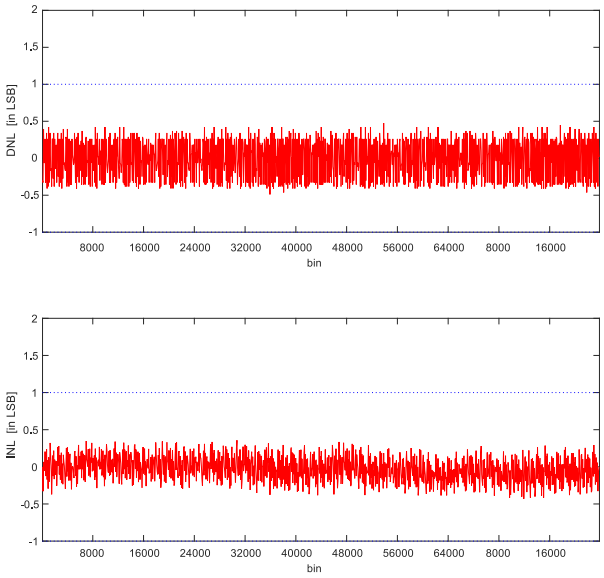

Fig. 14: Measured DNL and INL of ADC at 125 MS·s^{-1} after Calibration.

SNDR, but this ADC has based on foreground factory digital calibration to correct for capacitor mismatches, that's a onetime process only. The ADC presented in [23] is based on a novel calibration technique with

an auxiliary error amplifier and sign-sign LMS adaption. The problem comes with this ADC, when it has to operate on high sampling frequencies. The ADC used in [24] proved the viability of a low distortion 16-bit Pipelined ADC with sampling rate of 100 MS·s^{-1} to 160 MS·s^{-1} with SiGe BiCMOS process technology. The quite large power consumption and complicated implementation are major problems with this published ADC. The ADC presented in [25] is based on the study of the stage scaling theory. In this ADC, to implement a low power technique, residual amplifiers have been shared by two cascading MDACs. High value of INL and low value of SNDR are drawbacks of this Pipelined ADC. In [26], to reduce power consumption, double sampling MDAC and amplifier sharing techniques have been used. This low resolution 10-bit ADC with low values of SNDR and SFDR is only suitable for Video applications. From the comparison table, it's clear that the static and dynamic performance of the proposed Pipelined ADC are better than those published Pipelined ADCs, which operates from a supply voltage of 1.8 V, resolution of 16 bit and using CMOS process technology.

6. Conclusion

A 16-bit 125 MS·s^{-1} Pipelined ADC of Multi bit stage, without SHA in front-end, is described in this paper. The first and second stage of the 16-bit Pipelined ADC are of 3.5 bits, the succeeding stages from third to seventh are of 2.5 bits per stage, and a 3-bit flash ADC is used as the last stage of ADC. After bit alignment and truncation of 19 bits from all stages, the final digital output has achieved the 16-bit size. To improve ADC performance, the method of voltage reference separation has been used, which is really effective to prevent the kickback and settling within the available settling time. High gain Op-amp has been used in this design at each stage to remove nonlinear errors and capacitor mismatching. A combination of the two techniques of signal-dependent dithering and butterfly shuffler are used in the first two stages as a digital background calibration technique to remove linear errors. For the proposed ADC, the total power consumption is 300 mW. The DNL has improved from +1/-1 to 0.57/-0.48 and INL has improved from 8.7/-8.8 to 0.5/-0.5 after calibration. Due to the proposed calibration technique, SFDR has achieved a value of 97.74 dB and SNDR of 79.77 dB, when sampling with a 30 MHz full scale input at 125 MS·s^{-1}. The values of SFDR and SNDR achieved by sampling with a 150 MHz input are 88.9 dB and 73.5 dB respectively.

Acknowledgment

The authors of this paper would especially like to thank the reviewers for their precious time to give their expert comments. Per their valuable suggestions changes have been incorporated into the final version of this manuscript.

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