Analysis and Sliding Mode Control of Four-Wire Three-Leg Shunt Active Power Filter

Farid HAMOUDI, Hocine AMIMEUR

Laboratory of Renouwable Energies Mastering, Department of Electrical Engineering, Faculty of Technology, University of Bejaia, Bejaia, 06000, Algeria

f_hamoudi@yahoo.fr, hocineamimeur@gmail.com

DOI: 10.15598/aeee.v13i5.1344

Abstract. *In this paper, the analysis and the sliding mode control application for a shunt active filter is presented. The active filter is based on a three-leg split-capacitor voltage source inverter which is used to compensate harmonics and unbalance in the phase currents, and therefore to cancel neutral current. The proposed sliding mode control is formulated from the multivariable state model established in dq0 frames. The selection of the sliding mode functions takes in account simultaneously, the current tracking and the dc-bus regulation and balancing, without the need of outer loops for the dc-bus control. A particular attention is given to the sliding mode functions design in order to optimize the convergence of the zero-sequence error and the dc-bus voltage unbalance. The effectiveness of the proposed control has been verified through computer simulation where satisfactory results are obtained over different conditions.*

Keywords

Dc-bus voltage control, four-wire shunt active filter, harmonics current compensation, sliding mode control, Three-Leg Split-Capacitor VSI.

1. Introduction

Three-phase four-wire active power filters are nowadays one of the most popular solutions for power quality conditioning in four-wire distribution power systems [1].

The purpose of using a four-wire active power filter is to perform harmonic current suppression, reactive power compensation. In addition, the active filter is called to compensate load unbalance and to mitigate harmonic current in the neutral wire [2], [3], [4], [5], [6].

The implementation of such a filter usually uses a four-leg full bridge voltage source inverter that provides neutral current through the fourth leg [1], [2], or a three-leg split-capacitor voltage source inverter providing the neutral current through the fourth wire connected to midpoint of the dc-bus formed by two cascade connected capacitors [4]. This implementation can also be realized by three single-phase converters [6]. In the present paper the split-capacitor configuration is preferred especially for its reduced number of semi-conductors, which is economically and technically an advantage. However, for this configuration it is often difficult to compensate all zero-sequence currents, and to cancel perfectly the dc-bus unbalance simultaneously. This is due to the fact that all the zero-sequence compensated current flows through the dc-bus capacitors causing rise to voltage unbalance between the capacitors in that bus [4], [7]. This phenomenon is accentuated when compensated currents are highly distorted and unbalanced.

The control strategy is important to enhance the performances of the active filter. This control generally includes three steps: identification of the undesired components from the load currents, dc-bus voltage control and finally current tracking. A large number of control strategies have been reported in the literature for these different steps [8], [9], [10], [11], [12], [13]. However, for current tracking the sliding mode control seems to be the most appropriate because of the time varying nature of the converters [14], [15], [16], [17]. The main advantage of this kind of control resides in its very fast response, especially during the transient regimes even if the system state is so far to the desired surface. Consequently, the system dynamic is very high during the reaching phase. Furthermore, the simplicity and the robustness of the sliding mode for uncertain sys-

tems make it particularly attractive in despite of the chattering phenomenon [18], [19]. The sliding mode approach has proved its qualities for active filter applications in many contributions [20], [21], [22], [23], [24], [25]; however, most of these works deal with three-wire or four-wire four-leg active filters.

The dc-bus voltage control is of a crucial importance because it directly affects the performance of the active filter [26], [27], [28]. In case of the three-leg split-capacitor based active filter, this control consists in forcing the voltage source inverter to absorb additional currents from the mains to achieve voltage regulation and balancing in the dc-bus. Due to this effect the quality of the source current will depend strongly on the efficiency of the dc-bus control.

All along this paper, the attention is focused on the current tracking and the dc-bus control. A sliding mode control is proposed to control the three-leg four-wire shunt active filter. To formulate the sliding mode control, the space model of the active filter is developed in $dq0$ frames. The proposed approach in this paper avoids the use of multiple separate loops usually used to track the compensating currents and to regulate the dc-bus voltage. In fact, sliding mode functions are proposed to control the multivariable system as a whole including current tracking, dc-bus voltage regulation and dc-bus balancing. Thus the convergence of the state errors ensures all these objectives at the same time. Some difficulties have been encountered to satisfy simultaneously the zero-sequence tracking and dc-bus unbalance; however, by favoring the current convergence, this has been surmounted.

The layout of the paper is as follows: after this introduction, a description of the active filter is presented and a dynamic model is given. In section 3. , the active filter control is globally described while the aim contribution is presented in section 4. . The validation of the proposed control is carried out in section 5. through computer simulations under hard different load conditions. Finally the paper is ended by a conclusion.

2. Shunt Active Power Filter Description and Modeling

The three-phase four-wire active filter connected to the grid is shown in Fig. 1. The power circuit uses a three-leg voltage source inverter (VSI) coupled via inductor L_c which supposed to have a small internal resistance r_c. Two identical capacitors C are cascade connected to form the dc-side of the active filter. The midpoint of the dc-bus is connected to the neutral wire of the grid to form the fourth wire. The losses in each capacitor are represented by the resistance R. The nonlinear load

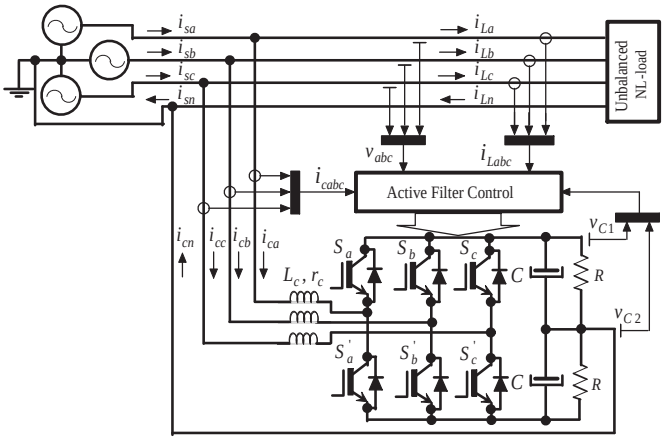

Fig. 1: Four-wire three-leg split capacitor shunt active filter.

is a combination of three-phase and single-phase rectifiers resulting in nonsinusoidal and unbalanced load current i_{Labc}. Therefore, a distorted current i_{Ln} flows in the neutral wire.

The role of the active filter can be resumed in two objectives: First, to inject in the point of common coupling three-phase compensating currents i_{cabc} to cancel harmonics from the three-phase currents in the source side i_{sabc} and to maintain the dc-bus voltage regulated at a predefined value. The second objectives is to inject a compensating current i_{cn} from the midpoint of the dc-bus to cancel the neutral source current i_{sn}, and to minimize voltage unbalance between the two capacitors of the dc-bus.
The dynamic model of the shunt active filter of Fig. 1 in $dq0$ reference frames can be expressed by the following differential equations:

$$
\begin{aligned}
L_c\frac{\mathrm{d}i_{cd}}{\mathrm{d}t} &= v_d - r_c i_{cd} + L_c\omega i_{cq} - \frac{v_{dc}}{2}u_d - \frac{\Delta v_{dc}}{2},\\
L_c\frac{\mathrm{d}i_{cq}}{\mathrm{d}t} &= v_q - r_c i_{cd} - L_c\omega i_{cd} - \frac{v_{dc}}{2}u_q - \frac{\Delta v_{dc}}{2},\\
L_c\frac{\mathrm{d}i_{c0}}{\mathrm{d}t} &= v_0 - r_c i_{c0} - \frac{v_{dc}}{2}u_0 - \frac{\sqrt{3}}{2}\Delta v_{dc},\\
C\frac{\mathrm{d}v_{dc}}{\mathrm{d}t} &= -\frac{1}{R}v_{dc} + u_d i_{cd} + u_q i_{cq} + u_0 i_{c0},\\
C\frac{\mathrm{d}\Delta v_{dc}}{\mathrm{d}t} &= -\frac{1}{R}\Delta v_{dc} + \sqrt{3}i_{c0},
\end{aligned}
\tag{1}
$$

where i_{cd}, i_{cq}, i_{c0} denote the $dq0$-axis compensating currents, v_{dc}, the total dc-bus voltage, i.e $v_{C1} + v_{C2}$ and Δv_{dc}, the dc bus voltage difference, i.e $v_{C1} - v_{C2}$. The $dq0$ voltages at the point of common coupling are denoted by v_d, v_q and v_0. ω represents the fundamental pulsation of the mains voltage, and finally u_d, u_q, u_0 denote the control variables of the system.

3. SAPF Control

In order to compensate correctly the undesired component, the references for active filter ac currents i_{cd}, i_{cq}, and i_{c0} must be identified first. A large number of contributions dealing with the computation of reference currents can be found in literature. The most common way is the time-based extracting from the load current, indirectly by using the pq-theory or directly by using the synchronous method [13]. The last one seems more adequate since the state model and the control are designed in the $dq0$ frames. The principle of this method consists in transforming the abc load currents to $dq0$ load current at the fundamental frequency i_{Ld}, i_{Lq}, and i_{L0}, then except the continuous component on the d axis $\bar{i}_{Lq}$, all the other components are to be compensated, or in other words, to be injected in the opposite phase. Thus, the current references in $dq0$ frames are $i^*_{cd} = -\tilde{i}_{Ld}$, $i^*_{cq} = -i_{Lq}$, and $i^*_{c0} = -i_{L0}$. In addition to these currents, necessary to cancel the harmonics and reactive power of the load, the active filter absorbs an additional active current to compensate its losses and to regulate dc-bus voltage v_{dc}. This current is usually determined by a PI controller in outer loop which computes an additional active current added to the reference current on the d axis. As particularity for the split-capacitor active filter, the dc-bus balancing is also necessary to ensure compensation objectives [4], [8], [24], [26]. In fact, if the active filter is called to compensate zero-sequence current, one must expect a dc-bus unbalance as shown by the last subequation in Eq. (1). This unbalance manifests as ripple which may contain average component. Consequently, a dc-term can be observed in the source currents, which increases certainly the THDs of the compensated currents. However, the same equation shows that, if the unbalance Δv_{dc} is forced to zero, the compensating zero-sequence current is also forced to zero, and then the neutral source current cannot be canceled, which contradicts the main objective. Thus, as conclusion, a compromise is necessary in the control design, by authorizing an acceptable ripple and possibly a slight dc-offset in dc-bus, all with compensating all the zero-sequence current.

4. Sliding Mode Control

For the formulation of the control design, the nonlinear multi-input multi-output (MIMO) model in Eq. (1) is rewritten as follows [15]:

$$\begin{aligned} \dot{\boldsymbol{x}} &= \boldsymbol{f}(\boldsymbol{x}) + \boldsymbol{G}(\boldsymbol{x})\boldsymbol{u}, \\ \boldsymbol{y} &= \boldsymbol{h}(\boldsymbol{x}), \end{aligned} \tag{2}$$

where $\boldsymbol{x} = [i_{cd} \;\; i_{cq} \;\; i_{c0} \;\; v_{dc} \;\; \Delta v_{dc}]^T \in \mathbb{R}^5$ represents the system state vector, $\boldsymbol{u} = [u_d \;\; u_q \;\; u_0]^T \in [-1,1]^3$ is the system control vector, $\boldsymbol{y} = [i_{cd} \;\; i_{cq} \;\; i_{c0}]^T \in \mathbb{R}^3$ is the system output vector. The function $\boldsymbol{f}(\boldsymbol{x}) \in \mathbb{R}^5$ is a smooth vector usually addressed as the drift vector field, and $\boldsymbol{G}(\boldsymbol{x}) \in (\mathbb{R}^5 \times \mathbb{R}^3)$ is called the input matrix, whose columns represent also smooth vector fields. Thereafter, the expressions of $\boldsymbol{f}(\boldsymbol{x})$ and $\boldsymbol{G}(\boldsymbol{x})$ are:

$$\boldsymbol{f}(\boldsymbol{x}) = \begin{pmatrix} (2v_d - 2r_c i_{cd} + 2L_c\omega i_{cq} - \Delta v_{dc})/2L_c \\ (2v_q - 2r_c i_{cq} - 2L_c\omega i_{cd} - \Delta v_{dc})/2L_c \\ (2v_0 - 2r_c i_{c0} - \sqrt{3}\Delta v_{dc})/2L_c \\ -v_{dc}/CR \\ -(\Delta v_{dc} - \sqrt{3}Ri_{c0})/CR \end{pmatrix}, \tag{3}$$

$$\boldsymbol{G}(\boldsymbol{x}) = \begin{pmatrix} -v_{dc}/2L_c & 0 & 0 \\ 0 & -v_{dc}/2L_c & 0 \\ 0 & 0 & -v_{dc}/2L_c \\ i_{cd}/C & i_{cq}/C & i_{c0}/C \\ 0 & 0 & 0 \end{pmatrix}. \tag{4}$$

To design the sliding mode control of the shunt active filter, recalling that the objective of this control is to track the reference currents on the axes $dq0$; i^*_{cd}, i^*_{cq} and i^*_{c0}, and to maintain the absolute voltage v_{dc} across the dc-bus constant in the steady state at its reference value v^*_{dc}, and finally to reduce as much as possible the dc-bus voltage difference Δv_{dc} without affecting the compensation of the zero-sequence current.

To accomplish the above mentioned objectives, we design three sliding mode functions with proportional actions as follows:

$$\boldsymbol{\sigma} = \begin{pmatrix} \sigma_d \\ \sigma_q \\ \sigma_0 \end{pmatrix} = \boldsymbol{K}(\boldsymbol{x}^* - \boldsymbol{x}), \tag{5}$$

where $\boldsymbol{K} = \begin{pmatrix} k_1 & 0 & 0 & k_2 & 0 \\ 0 & k_1 & 0 & 0 & 0 \\ 0 & 0 & k_1 & 0 & k_3 \end{pmatrix}$, k_1, k_2 and k_3 are postives gains, $\boldsymbol{x}^* = [i^*_{cd} \;\; i^*_{cq} \;\; i^*_{c0} \;\; v^*_{dc} \;\; \Delta v^*_{dc}]^T$ is the reference vector.

The sliding mode function on the d-axis takes in account the i^*_{cd} tracking, and the dc-bus voltage v_{dc} regulation. Notice that this regulation, represented by the second term in σ_d is often done by forcing the active filter to absorb or to inject an additional active current from or into the mains. The sliding mode function σ_q is to track the reference i^*_{cq}, and finally, on 0-axis, the sliding mode function will be used to track the reference currents on that axis and to control the dc-bus voltage difference Δv_{dc}. Reformulating the problem, the objective now is to force the function $\boldsymbol{\sigma}$ to zero, thanks to the control actions $\boldsymbol{u}$. In other words, to force the state trajectory to evolve over the sliding surface S given by:

$$S = \{\boldsymbol{x} \in \mathbb{R}^5 | \boldsymbol{\sigma} = \boldsymbol{0}\}, \tag{6}$$

This objective is usually obtained by using a control law of the form:

$$\boldsymbol{u} = \hat{\boldsymbol{u}} + \boldsymbol{u}_{eq}, \tag{7}$$

where $\hat{\boldsymbol{u}} = -\text{sign}(\boldsymbol{\sigma})$ is a switching component that pulls the trajectory towards the sliding surface, and $\boldsymbol{u}_{eq}$ is a smooth component that approximates a control law where the net change of the sliding surface is zero, then the last component is valid only on the sliding surface S.

4.1. Equivalent Control

The existence of the sliding mode control is conditioned by the existence of the sliding mode equivalent control. Assume that after a certain time, through the control actions, the state of the system reaches the surface defined by $\boldsymbol{\sigma} = \mathbf{0}$ and stays on it at any time. Thus, the time derivative of the switching mode function $\dot{\boldsymbol{\sigma}}$ must be also zero, and then, the following invariance condition is driven

$$\dot{\boldsymbol{\sigma}} = \frac{\partial \boldsymbol{\sigma}}{\partial \boldsymbol{x}^T}(\dot{\boldsymbol{x}}^* - \dot{\boldsymbol{x}}) = 0, \tag{8}$$

which can be written as:

$$\frac{\partial \boldsymbol{\sigma}}{\partial \boldsymbol{x}^T}\Big(\dot{\boldsymbol{x}}^* - \boldsymbol{f}(\boldsymbol{x}) - \boldsymbol{G}(\boldsymbol{x})\boldsymbol{u}\Big) = 0. \tag{9}$$

If this condition stills verified after reaching the sliding surface, then by solving Eq. (9) for $\boldsymbol{u}$, a smooth control law defined as the equivalent control can be imagined and established as follows:

$$\boldsymbol{u}_{eq} = [\boldsymbol{L_G}(\boldsymbol{x})]^{-1}\Big(\boldsymbol{K}\dot{\boldsymbol{x}}^* - \boldsymbol{l_f}(\boldsymbol{x})\Big), \tag{10}$$

where, $\boldsymbol{L_G}(\boldsymbol{x}) = \dfrac{\partial \boldsymbol{\sigma}}{\partial \boldsymbol{x}^T}\boldsymbol{G}(\boldsymbol{x}) = \boldsymbol{K}\boldsymbol{G}(\boldsymbol{x})$, $\boldsymbol{l_f}(\boldsymbol{x}) = \dfrac{\partial \boldsymbol{\sigma}}{\partial \boldsymbol{x}^T}\boldsymbol{f}(\boldsymbol{x}) = \boldsymbol{K}\boldsymbol{f}(\boldsymbol{x})$. As stated above, this smooth control is only defined when $(\boldsymbol{\sigma}, \dot{\boldsymbol{\sigma}}) = (\mathbf{0}, \mathbf{0})$, then it is valid only on the sliding surface, and can be seen as the approximation of the control $\boldsymbol{u}$ where the net change of the sliding surface around this one tends to zero.

To ensure the equivalent control existence, one must ensure that the matrix $\boldsymbol{L_G}(x)$ is invertible. This one is given by:

$$\boldsymbol{L_G}(\boldsymbol{x}) = \begin{pmatrix} -\frac{k_1 v_{dc}}{2L_c} + \frac{k_2 i_{cd}}{C} & \frac{k_2 i_{cq}}{C} & \frac{k_2 i_{c0}}{C} \\ 0 & -\frac{k_1 v_{dc}}{2L_c} & 0 \\ 0 & 0 & -\frac{k_1 v_{dc}}{2L_c} \end{pmatrix}. \tag{11}$$

Thus, as condition for equivalent control existence, all the diagonal entries must be non zero, then, one can write:

$$-\frac{k_1 v_{dc}}{2L_c} + \frac{k_2 i_{cd}}{C} \neq 0. \tag{12}$$

Moreover, each entry in the equivalent control vector must be bounded within [-1,1].

4.2. Sliding Mode Stability

To ensure sliding mode stability, the Lyapunov's approach is often used [15], [30], [31]. In this way, let suppose the following candidate function:

$$V(\boldsymbol{\sigma}) = \frac{1}{2}\boldsymbol{\sigma}^T\boldsymbol{\sigma}. \tag{13}$$

To ensure sliding mode stability the function V must verify the following conditions:

$$\begin{cases} V(\boldsymbol{\sigma}) = 0 & \text{if} \quad \boldsymbol{\sigma} = \mathbf{0}, \\ V(\boldsymbol{\sigma}) > 0 & \text{if} \quad \boldsymbol{\sigma} \neq \mathbf{0}, \\ \dot{V}(\boldsymbol{\sigma}) < 0 & \text{if} \quad \boldsymbol{\sigma} \neq \mathbf{0}, \\ V(\boldsymbol{\sigma}) \to \infty & \text{if} \quad |\boldsymbol{\sigma}| \to \infty. \end{cases} \tag{14}$$

The quantity V represents the distance of the state $\boldsymbol{x}$ to the sliding surface S. This distance is precisely zero over the surface, i.e when $\boldsymbol{\sigma} = \mathbf{0}$ and positive otherwise, i. e. when $\boldsymbol{\sigma} \neq \mathbf{0}$. In addition, this distance tends to infinity when $|\boldsymbol{\sigma}|$ tends to infinity. Thus, a sufficient condition for the stability in the sliding mode operation is that, when the distance V is not zero, it must be decreased. In other words, when $V(\boldsymbol{\sigma}) > 0$, its time derivative must be negative, then one can write the necessary condition for the sliding mode stability as:

$$\dot{V}(\boldsymbol{\sigma}) = \boldsymbol{\sigma}^T\dot{\boldsymbol{\sigma}} < 0. \tag{15}$$

Substituting Eq. (9) in Eq. (15):

$$\boldsymbol{\sigma}^T\frac{\partial \boldsymbol{\sigma}}{\partial \boldsymbol{x}^T}\Big(\dot{\boldsymbol{x}}^* - \boldsymbol{f}(\boldsymbol{x}) - \boldsymbol{G}(\boldsymbol{x})\boldsymbol{u}\Big) < 0. \tag{16}$$

In other form:

$$\boldsymbol{\sigma}^T\Big(\boldsymbol{K}\dot{\boldsymbol{x}}^* - \boldsymbol{l_f}(\boldsymbol{x}) - \boldsymbol{L_G}(\boldsymbol{x})(\hat{\boldsymbol{u}} + \boldsymbol{u}_{eq})\Big) < 0. \tag{17}$$

Substituting Eq. (10) in Eq. (17) the following condition is driven

$$-\boldsymbol{\sigma}^T\boldsymbol{L_G}(\boldsymbol{x})\hat{\boldsymbol{u}} < 0, \tag{18}$$

After development, this condition is written as:

$$\begin{aligned} &\sigma_d\Big(-\frac{k_1 v_{dc}}{2L_c}\text{sgn}(\sigma_d) + \frac{k_2 i_{cd}}{C}\text{sgn}(\sigma_d) + \\ &+\frac{k_2 i_{cq}}{C}\text{sgn}(\sigma_q) + \frac{k_2 i_{c0}}{C}\text{sgn}(\sigma_0)\Big) + \\ &-\sigma_q\frac{k_1 v_{dc}}{2L_c}\text{sgn}(\sigma_q) - \sigma_0\frac{k_1 v_{dc}}{2L_c}\text{sgn}(\sigma_0) < 0. \end{aligned} \tag{19}$$

This can be rewritten more adequately as:

$$\begin{aligned} &-\sigma_d\text{sgn}(\sigma_d)\Big(\frac{k_1 v_{dc}}{2L_c} - \frac{k_2 i_{cd}}{C} - \frac{k_2 i_{cq}}{C}\frac{\text{sgn}(\sigma_q)}{\text{sgn}(\sigma_d)} + \\ &-\frac{k_2 i_{c0}}{C}\frac{\text{sgn}(\sigma_0)}{\text{sgn}(\sigma_d)}\Big) + \\ &-\sigma_q\text{sgn}(\sigma_q)\Big(\frac{k_1 v_{dc}}{2L_c}\Big) - \sigma_0\text{sgn}(\sigma_0)\Big(\frac{k_1 v_{dc}}{2L_c}\Big) < 0. \end{aligned} \tag{20}$$

Since $\sigma_k \text{sgn}(\sigma_k)$ and v_{dc} are positive, the last condition can be restricted to:

$$\frac{k_1 v_{dc}}{2L_c} - \frac{k_2 i_{cd}}{C} - \frac{k_2 i_{cq}}{C}\frac{\text{sgn}(\sigma_q)}{\text{sgn}(\sigma_d)} - \frac{k_2 i_{c0}}{C}\frac{\text{sgn}(\sigma_0)}{\text{sgn}(\sigma_d)} > 0. \tag{21}$$

then

$$\frac{k_1}{k_2} > \frac{2L_c}{C}\frac{i_{cd} + i_{cq}\frac{\text{sgn}(\sigma_q)}{\text{sgn}(\sigma_d)} + i_{c0}\frac{\text{sgn}(\sigma_0)}{\text{sgn}(\sigma_d)}}{v_{dc}}. \tag{22}$$

Which can be always verified by choosing the gains k_1 and k_2 such that:

$$\frac{k_1}{k_2} > \frac{2L_c}{C}\frac{|i_{cd}| + |i_{cq}| + |i_{c0}|}{v_{dc}}. \tag{23}$$

According to Eq. (19), we can see that $\dot{V}(\boldsymbol{\sigma}) < 0$, which implies the attractiveness of the sliding surface. Moreover, we can see that $\lim_{\boldsymbol{\sigma}\to\mathbf{0}} \dot{V}(\boldsymbol{\sigma}) = 0$, and then the surface is invariant.

When the sliding mode occurs, $\boldsymbol{\sigma} = \mathbf{0}$, the tracking behavior of the system dynamics on the d-axis is determined by the following equations:

$$i^*_{cd} - i_{cd} = -\frac{k_2}{k_1}(v^*_{dc} - v_{dc}). \tag{24}$$

Thus, the dc-bus voltage convergence is proportional to the current convergence on the d-axis. However, it is preferable to set k_1 enough larger than k_2 to ensure fast convergence of the current. The condition Eq. (23) shows that the sliding mode stability is independent of the gain k_3. Effectively, it has been observed through simulation tests that this gain does not affect the stability. However, the zero-sequence current tracking and the dc-bus unbalance are directly affected. To design this gain, let us consider the following equation, valid when the sliding mode occurs:

$$i^*_{c0} - i_{c0} = \frac{k_3}{k_1}\Delta v_{dc}. \tag{25}$$

Notice that it is assumed that $\Delta v^*_{dc} = 0$. In this equation the gain k_1 is already fixed, thus, if $k_3 > k_1$, the convergence of Δv_{dc} is faster than the convergence of $(i^*_{c0} - i_{c0})$. This will result in very small dc-bus unbalance ($\Delta v_{dc} \to 0$), but it is not the case for $(i^*_{c0} - i_{c0})$. If $k_3 << k_1$, the convergence of $(i^*_{c0} - i_{c0})$ is faster, and will result in perfect zero-sequence current tracking ($i_{s0} \to 0$), but a significant ripple and dc-offset remains in Δv_{dc}. Thus a possible strategy to design the gain k_3 consists in allowing an admissible dc-bus unbalance $(\Delta v_{dc})_{adm}$ (for example 5% of v_{dc}), and a small current error $(\varepsilon_0)_{adm} = i^*_{c0} - i_{c0}$, and then in ensuring convergence of Eq. (25) to the point $((\varepsilon_0)_{adm}, (\Delta v_{dc})_{adm})$. Thus the gain k_3 can be chosen as follows:

$$k_3 = \frac{|\varepsilon_0|_{adm}}{|\Delta v_{dc}|_{adm}} k_1. \tag{26}$$

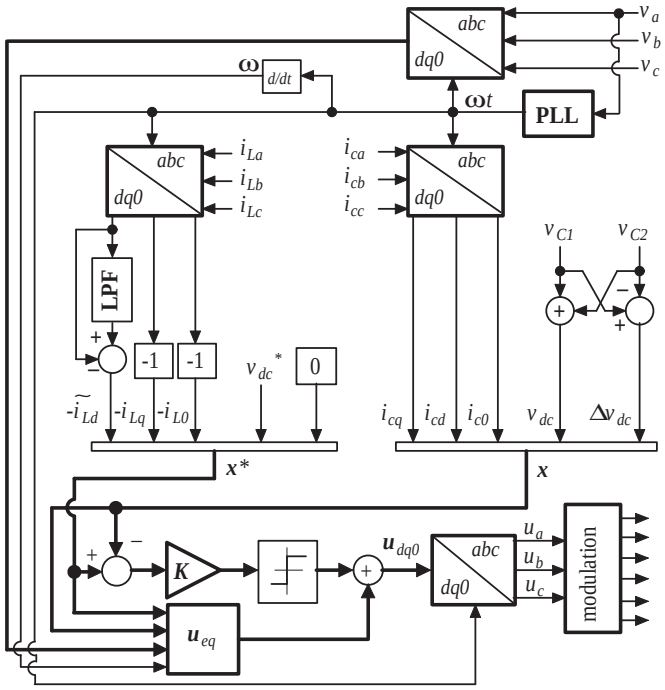

Fig. 2: Control block diagram of the shunt active filter.

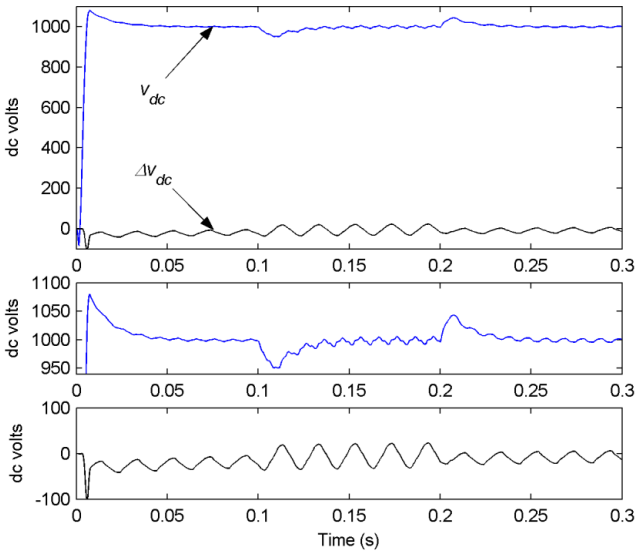

Fig. 3: dc-bus voltage; total voltage v_{dc} (zoom), and voltage unbalance Δv_{dc} (zoom) ($\alpha = 0°$).

It is clear that the zero-sequence tracking error is necessary to design k_3. Equation (26) shows also that naturally $k_3 < k_1$, then zero-sequence error converges faster than dc-bus unbalance.

5. Results and Discussion

The effectiveness of the proposed control has been verified through computer simulations. The system parameters are given in the appendix. The load is con-

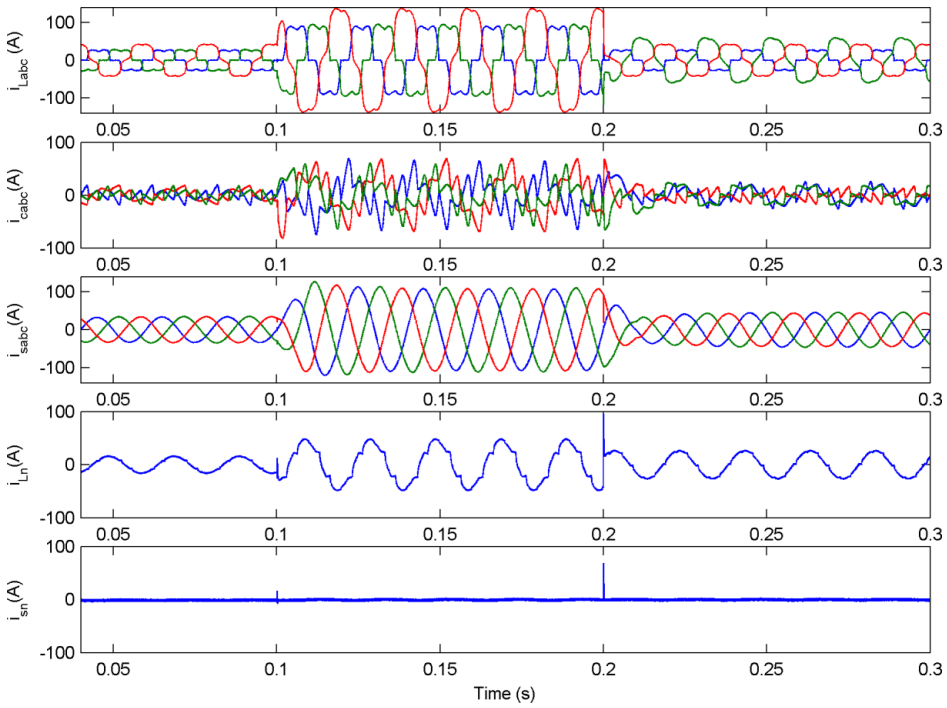

Fig. 4: From the top to the bottom; three-phase load current, three-phase compensating current, three-phase source current, neutral load current and finally, neutral source current ($\alpha = 0°$).

stituted in a three-phase thyristor rectifier and single phase diode rectifiers, resulting in nonsinusoidal and unbalanced currents. The system control diagram is represented in Fig. 2. Two simulation tests are carried out; In the first test, the firing angle α of the thyristor rectifier is set to zero. For the second test this angle is set to 45°, increasing therfore the THDs of the drawn currents. For the both tests, two load changes are voluntarily created at 0.1 and 0.2 s to verify the tracking performances.

5.1. Simulation Results ($\alpha = 0°$)

The dc-bus total voltage and unbalance are shown in Fig. 3. First, one can observe a very fast dynamic response during the transient state. When the load current increases suddenly, the dc-bus voltage decreases, and when the load current decreases this voltage increases. However, in both cases this voltage variation does not exceed 4 % of v_{dc}. Moreover, it reaches the reference value in very short time (about one cycle). During the steady state a slight ripple (about 5 V) endures in v_{dc}, but the average value stays constant and equal to the reference value. The dc-bus unbalance Δv_{dc} is also, satisfactory. Although, during a transient period, the average value of this unbalance is not zero, its magnitude is insignificant (about 20 V). Moreover, this dc-term goes gradually to zero, and only a small ripple (less than 3 % of v_{dc}) remains after about 0.12 sec.

Load, active filter and source currents are shown in Fig. 4. The load currents are nonsinusoidal and unbalanced resulting in neutral current. It can be seen that the proposed control is able to force the compensating current to track their references, during steady state and when the load changes. Thus, the objective of sinusoidal phase currents and canceled neutral one at the source side is ensured for different states of the load. In fact, in all cases the resulting THDs are less than 1.5 %,

Tab. 1: Summarized simulation results obtained for $\alpha = 0°$.

Time		$0 < t < 0.1$ sec				$0.1 < t < 0.2$ sec				$0.2 < t < 0.3$ sec			
phase		**a**	**b**	**c**	**N**	**a**	**b**	**c**	**N**	**a**	**b**	**c**	**N**
RMS (A)	**Load**	19.95	20.53	32.03	11.19	66.31	68.90	102.4	32.79	20.06	43.27	31.91	18.63
	Source	23.89	24.18	24.00	00.30	75.96	76.94	76.05	00.62	31.82	31.95	31.37	00.35
THD (%)	**Load**	27.64	26.47	16.16	05.03	23.41	23.34	13.87	12.29	27.58	12.21	16.27	05.72
	Source	01.14	01.07	01.10	30!	01.16	01.24	01.11	05.50	01.49	01.48	01.53	03.39
Neq-seq (%)	**Load**	17.12				15.63				23.01			
	Source	01.08				01.02				01.55			
Zer-seq (%)	**Load**	15.51				13.79				19.58			
	Source	00.35				00.23				00.40			

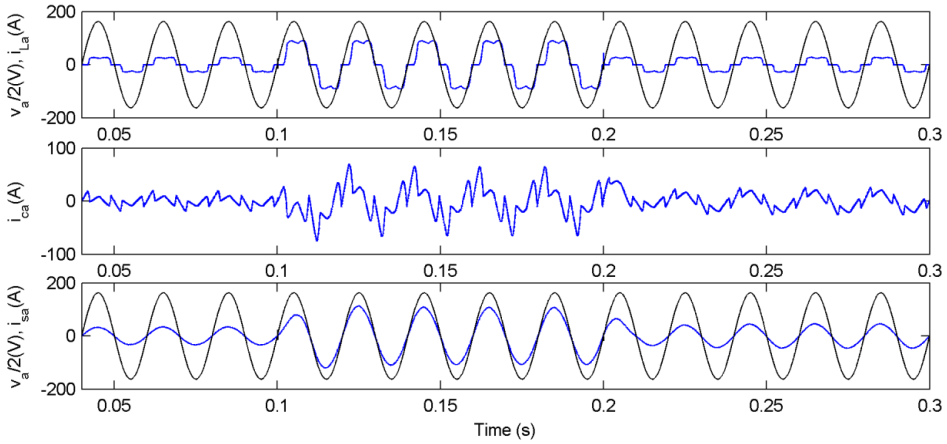

Fig. 5: From the top to the bottom; a-phase load current and voltage (50% of v_a), a-phase compensating current, a-phase source current and voltage (50% of v_a) ($\alpha = 0°$).

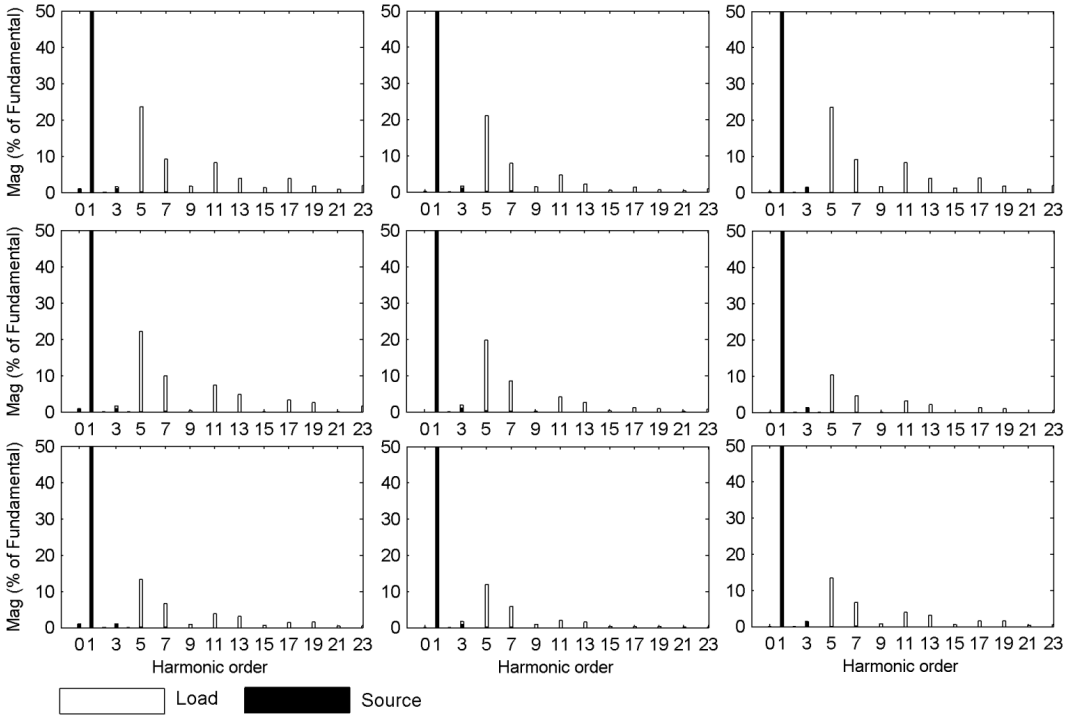

Fig. 6: Current spectrums; from top to bottom, phases a, b and c. From left to right; before load change, after the first load change, and finally after the second load change ($\alpha = 0°$).

and the RMS value is almost the same for each phase. For more details, the THD, the RMS values are summarized in Tab. 1, as well as the negative-sequence and the zero-sequence rates for different load conditions. The negative and zero-sequence rates are insignificant in the source currents; therefore, these currents are well balanced. Furthermore, in Fig. 5, the a-phase current and voltage are represented, to show that the source current is also in phase to the corresponding voltage.

Figure 6 shows current spectrums for different load changes. These spectrums show that the whole undesired harmonics are well canceled. However, during the period [0, 0.1 s], one can observe that a slight dc-term (harmonic 0) appears. This is due to the fact that during this period the dc-bus unbalance has non-zero average value. Notice also that due the dc-bus ripple, the third harmonic seems to be remaining, but with small value (about 1.5 %).

5.2. Simulation Results ($\alpha = 45°$)

During this test, the firing angle is voluntarily increased to observe the effectiveness of the control under hard polluted load currents. The different results are shown in Fig. 7, Fig. 8, Fig. 9 and Fig. 10. Naturally, the load currents are now more distorted, resulting in

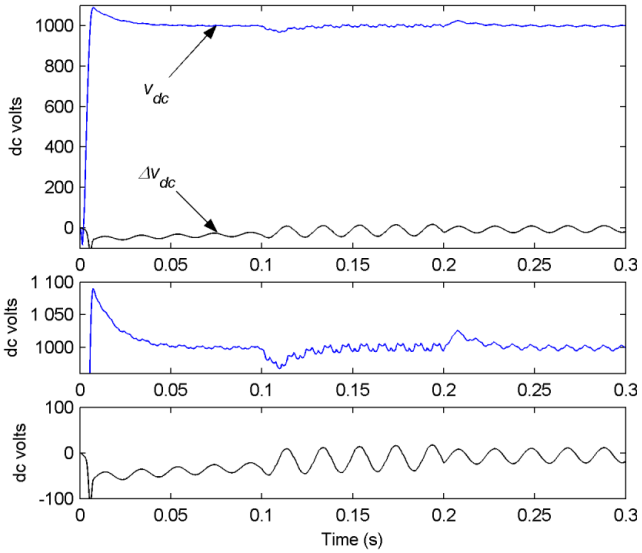

Fig. 7: dc-bus voltage; total voltage v_{dc} (zoom), and voltage unbalance Δv_{dc} (zoom) ($\alpha = 45°$).

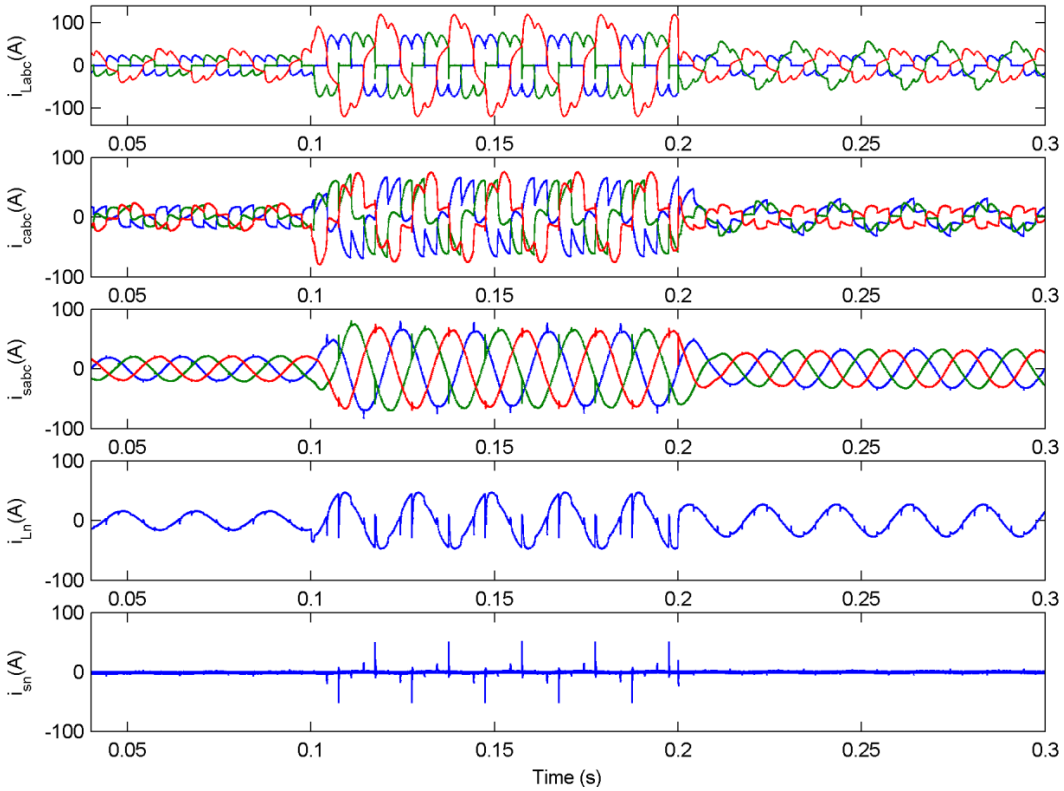

Fig. 8: From the top to the bottom; three-phase load current, three-phase compensating current, three-phase source current, neutral load current and finally, neutral source current ($\alpha = 45°$).

increased THDs; however, one can observe that almost the same performances are conserved as in the first test. The dc-bus voltage control conserves the same dynamic reponse during transient regime and against load change. It should be noticed that the dc-bus unbalance is relatively more significant during the transient regime, but remains acceptable (about 40 V) and it tends gradually to zero. For the phase and neutral currents, satisfactory results are also observed as shown in Fig. 8. All the THDs are less then 3.5 %, which agrees with the IEEE 519 standards. The currents spectrums in Fig. 10 show that the whole harmonics are canceled, and the dc-term appearing for $t < 0.1$ s remains acceptable. The detailled results for this test are recapitulated in Tab. 2.

Tab. 2: Summarized simulation results obtained for $\alpha = 45°$.

Time		$0 < t < 0.1$ sec				$0.1 < t < 0.2$ sec				$0.2 < t < 0.3$ sec			
phase		**a**	**b**	**c**	**N**	**a**	**b**	**c**	**N**	**a**	**b**	**c**	**N**
RMS (A)	**Load**	14.36	14.50	24.90	11.06	48.47	49.56	78.38	31.04	14.51	34.94	24.94	24.86
	Source	14.40	14.67	14.48	00.32	45.17	45.48	44.93	01.02	22.54	22.64	22.00	00.35
THD (%)	**Load**	37.10	37.79	19.95	06.55	31.93	33.09	18.35	21.81	36.80	15.15	20.33	06.13
	Source	02.21	02.09	02.17	33.6!	03.45	03.09	01.86	181	02.53	02.36	02.36	32.2
Neq-seq (%)	**Load**	22.87				19.60				29.83			
	Source	01.73				01.59				02.21			
Zer-seq (%)	**Load**	20.88				17.49				25.27			
	Source	00.63				00.70				00.47			

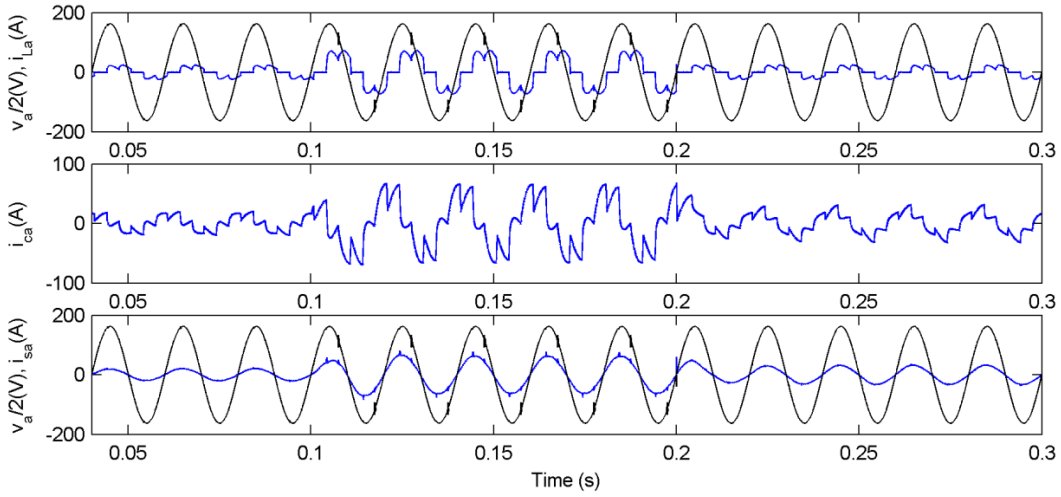

Fig. 9: From the top to the bottom; a-phase load current and voltage (50% of v_a), a-phase compensating current, a-phase source current and voltage (50% of v_a) ($\alpha = 45°$).

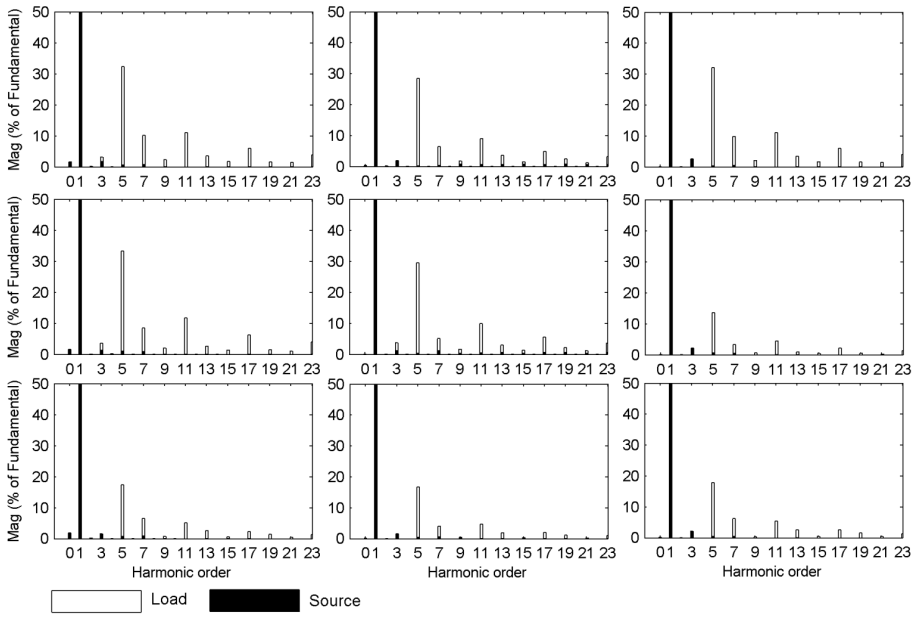

Fig. 10: Current spectrums; from top to bottom, phases a, b and c. From left to right; before load change, after the first load change, and finally after the second load change ($\alpha = 45°$).

6. Conclusion

The work presented in this paper proposes a sliding mode control for a three-leg voltage source inverter based four-wire active filter. The difficulties of the dc-bus voltage control in a split-capacitor active filter have been analyzed. The developed sliding mode control was aimed to be able to track compensating cur-

rent reference, and to regulate the dc-bus voltage and unbalance simultaneously. All this without using any control loop for the dc-bus voltage. The performances of the proposed control have been studied under various conditions. The obtained results have shown very satisfactory performances to track the compensating reference currents and to reduce THDs of the source currents, and therefore to ensure a sinusoidal balanced current and a zero neutral current, even under hard polluted nonlinear currents. It is also shown that the controller is able to ensure very high dc-bus voltage dynamic in the transient state, and against load change. During the steady state, excellent dc-bus voltage regulation has also been observed. Furthermore, the proposed control was able to make a compromise between the zero-sequence current tracking and dc-bus voltage unbalance compensation.

Appendix

Tab. 3: Simulated system parameters.

AC source	$V_{rms} = 230$ V, f=50 Hz
	$r_s = 1$ mΩ, L_s=20 μH
Active Filter	L_c=1 mH, $r_c = 0.5$ mΩ
	$C = 5$ mF, R=2 kΩ
	$v^*_{dc} = 1000$ V
SM gains	$k_1 = 2.1$, $k_2 = 0.85$, $k_3 = 0.02$
PWM frequency	12.5 kHz

References

[1] SINGH, B., K. AL-HADDAD and A. CHANDRA. A review of active filters for power quality improvement. *IEEE Transaction on Industrial Electronics*. 1999, vol. 46, iss. 5, pp. 960–971. ISSN 0278-0046. DOI: 10.1109/41.793345.

[2] QUINN, C. A. and N. MOHAN. Active filtering of harmonic currents in three-phase, four-wire systems with three-phase and single-phase nonlinear loads. In: *Applied Power Electronics Conference*. Boston: IEEE, 1992, pp. 829–836. ISBN 0-7803-0485-3. DOI: 10.1109/APEC.1992.228328.

[3] SINGH, B., K. AL-HADDAD and A. CHANDRA. Harmonic elimination, reactive power compensation and load balancing in three-phase, four-wire electric distribution systems supplying non-linear loads. *Electric Power System Research*. 1998, vol. 44, iss. 2, pp. 44–93. ISSN 0378-7796. DOI: 10.1016/S0378-7796(97)01187-5.

[4] LIN, B. R. and T. Y. YANG. Analysis and implementation of three-phase power quality compensator under the balanced and unbalanced load conditions. *Electric Power System Research*. 2006, vol. 76, iss. 5, pp. 271–282. ISSN 0378–7796. DOI: 10.1016/j.epsr.2005.05.010.

[5] PATNAIK, S. S. and A. K. PAND. Three-level h-bridge and three H-briges-based three-phase four-wire shunt active power filter topologies for high voltage applications. *International Journal of Electric Power and Energy Systems*. 2013, vol. 51, iss. 1, pp. 298–306. ISSN 0142–0615. DOI: 10.1016/j.ijepes.2013.02.037.

[6] GARCIA CAMPANHO, L. B., S. A. OLIVEIRA DA SILVA and A. GOEDTAL. Application of shunt active power filter for harmonic reduction and reactive power compensation in three-phase four-wire systems. *IET Power Electronics*. 2014, vol. 7, iss. 11, pp. 2825–2836. ISSN 1755-4535. DOI: 10.1049/iet-pel.2014.0027.

[7] CELANOVIC, N. and D. A. BOROYEVICH. Comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. *IEEE Transaction on Power Electronics*. 2000, vol. 12, iss. 2, pp. 242–249. ISSN 0885-8993. DOI: 10.1109/63.838096.

[8] AREDES, M., J. HAFNER and K. HEULMANN. Three-phase four-wire shunt active filter control strategies. *IEEE Transactions on Power Electronics*. 1997, vol. 12, iss. 2, pp. 311–318. ISSN 0885-8993. DOI: 10.1109/63.558748.

[9] BUSO, S., L. MALESANI and P. MATTAVELLI. Comparison of current control techniques for active filter applications. *IEEE Transactions on Industrial Electronics*. 1998, vol. 45, iss. 5, pp. 722–729. ISSN 0278-0046. DOI: 10.1109/41.720328.

[10] GREEN, T. C. and J. H. MARKS. Control techniques for active power filters. *IEE Electrical Power Applications*. 2005, vol. 152, iss. 2, pp. 369–381. ISSN 1350-2352. DOI: 10.1049/ip-epa:20040759.

[11] SINGH, B. N., B. SINGH, A. CHANDRA, P. RASTGOUFAR and K. AL-HADDAD. An improved control algorithm for active filters. *IEEE Transactions on Power Delivery*. 2007, vol. 22, iss. 2, pp. 1009–1020. ISSN 0885-8977. DOI: 10.1109/TPWRD.2006.886790.

[12] BRUCE, S. C. and G. JOOS. Direct power control of active filters with averaged switching frequency regulation. *IEEE Transactions on Power Electronics*. 2008, vol. 23, iss. 6, pp. 2729–2737. ISSN 0885-8993. DOI: 10.1109/TPEL.2008.2004958.

[13] ZAVERI, T., B. BHALJA and N. ZAVERI. Comparison of control strategies for dstatcom in three-phase, four-wire distribution system for power quality improvement under various source voltage and load conditions. *International Journal of Electrical Power and Energy systems*. 2012, vol. 43, iss. 1, pp. 582–594. ISSN 0142-0615. DOI: 10.1016/j.ijepes.2012.06.044.

[14] SPIAZZI, G., P. MATTAVELLI, L. ROSSETTO and L. ALESANI. Application of sliding mode control to

switch-mode power supplies. *Journal of Circuit Systems*. 1995, vol. 5, iss. 3, pp. 337–354. ISSN 0218-1266. DOI: 10.1142/S0218126695000217.

[15] SIRA-RAMIREZ, H. and R. SILVA-ORTIGOZA. *Control design techniques in power electronics devices*. London: Springer-Verlag, 2006. ISBN 978-1-84628-458-8.

[16] NAVARRO-LOPEZ, M., D. CORTES and C. CASTRO. Design of practical sliding-mode controllers with constant switching frequency for power converters. *Electric Power system Research*. 2009, vol. 79, iss. 5, pp. 796–802. ISSN 0378-7796. DOI: DOI: 10.1016/j.epsr.2008.10.018.

[17] TAN, S., Y. LAI and C. TSE. Implementation of pulse-widthmodulation based sliding mode controller for boost converters. *IEEE Transactions on Power Electronics*. 2006, vol. 3, iss. 4, pp. 130-135. ISSN 0885-8993. DOI: 10.1109/LPEL.2005.863269.

[18] VIEIRA, E., L. NUNES and F. LIZARRALDE. Global exact tracking for uncertain systems using output-feedback sliding mode control. *IEEE Transactions on Automation Control*. 2009, vol. 54, iss. 5, pp. 1141–1147. ISSN 0018-9286. DOI: 10.1109/TAC.2009.2013042.

[19] ZHANG, J. and Y. XIA. Design of static output feedback sliding mode control for uncertain linear systems. *IEEE Transactions on Industrial Electronics*. 2010, vol. 57, iss. 6, pp. 2161–2170. ISSN 0278-0046. DOI: 10.1109/TIE.2009.2033485.

[20] SAETIEO, S., R. DEVARAJ and D. A. TORREY. The design and implementation of a three-phase active power filter based on sliding mode control. *IEEE Transactions on Industrial Applications*. 1995, vol. 31, iss. 5, pp. 993–1000. ISSN 0093-9994. DOI: 10.1109/28.464511.

[21] LIN, B. R., Z. L. HUNG, S. C. TSAY and M. S. LIAO. Shunt active filter with sliding mode control. In: *International Conference on Electrical and Electronics Technology*. Singapor: IEEE, 2001, pp. 884–889. ISBN 0-7803-7101-1. DOI: 10.1109/TENCON.2001.949723.

[22] MENDALEK, N., K. AL-HADDAD, F. FNAIECH and L. A. DESSAINT. Sliding mode control of 3-phase 3-wire shunt active filter in the dq-frame. In: *International Conference on Electrical and Computer Engineering*. Toronto: IEEE, 2001, pp. 765–770. ISBN 0-7803-6715-4. DOI: 10.1109/CCECE.2001.933538.

[23] GUO, W. F., J. WU and D. G. XU. A novel sliding mode control of a high-voltage transformerless hybrid shunt active power filter. In: *International Conference on Industrial Electronics and Applications*. Xi'an: IEEE, 2009, pp. 2899–2904. ISBN 978-1-4244-2799-4. DOI: 10.1109/ICIEA.2009.5138741.

[24] HAMOUDI, F., A. A. CHAGHI, M. ADLI and H. AMIMEUR. A sliding mode control for four-wire shunt active filter. *Journal of Electrical Engineering-Slovak*. 2011, vol. 62, iss. 5, pp. 267–273. ISSN 1335-3632. DOI: 10.2478/v10187-011-0042-y.

[25] LU, W., L. CHUNWEN and X. CHANGBO. Sliding mode control of a shunt hybrid active power filter based on the inverse system method. *International Journal of Electrical Power and Energy systems*. 2014, vol. 57, iss. 5, pp. 39–48. ISSN 0142-0615. DOI: 10.1016/j.ijepes.2013.11.044.

[26] CHOI, W. H., C. S. LAM, M. C. WONG and Y. D. HAN. Analysis of DC-link voltage controls in three-phase four-wire hybrid active power filters. *IEEE Transactions on Power Electronics*. 2013, vol. 28, iss. 5, pp. 2180–2191. ISSN 0885-8993. DOI: 10.1109/TPEL.2012.2214059.

[27] LAM, C. S., W. H. CHOI, M. C. WONG and Y. D. HAN. Adaptive DC-link voltage-controlled hybrid active power filters for reactive power compensation. *IEEE Transactions on Power Electronics*. 2012, vol. 27, iss. 4, pp. 1758–1772. ISSN 0885-8993. DOI: 10.1109/TPEL.2011.2169992.

[28] SOLANO, O., C. VIVIESCAS, M. MANTILLA, J. PETIT and A. ACEVEDO. Experimental evaluation of dc bus voltage control in shunt active power filter with split capacitor using real time hardware in the loop simulation. In: *Electrical Power and Energy Conference (EPEC)*. Winnipeg: IEEE, 2011, pp. 398–403. ISBN 978-1-4577-0405-5. DOI: 10.1109/EPEC.2011.6070233.

[29] RAHMANI, S., N. MENDALEK and K. AL-HADDAD. Experimental design of a nonlinear control technique for three-phase shunt active power filter. *IEEE Transactions on Industrial Electronics*. 2010, vol. 57, iss. 10, pp. 3364–3375. ISSN 0278-0046. DOI: 10.1109/TIE.2009.2038945.

[30] RAHMANI, S., A. HAMADI and K. AL-HADDAD. A Lyapunov function-based control for a three-phase shunt hybrid active filter. *IEEE Transactions on Industrial Electronics*. 2012, vol. 59, iss. 3, pp. 1418–1429. ISSN 0278–0046. DOI: 10.1109/TIE.2011.2163370.

[31] HUA, C. C., C. H. LI and C. S. LEE. Control analysis of an active power filter using Lyapunov candidate. *IET Power Electronics*. 2008, vol. 2, iss. 4, pp. 325–334. ISSN 1755-4535. DOI: 10.1049/iet-pel.2008.0235.

About Authors

Farid HAMOUDI was born in Bejaia, Algeria on March 24, 1980. He received the engineer diploma in electrical engineering from the University of Bejaia in 2005. In 2008 and 2012, he received the M.Sc. and the Ph.D. degrees respectively from the University of Batna, Algeria. From 2009 to 2013, he was working

as a teacher at the Institute of Electrical Engineering and Electronics, Boumerdes, Algeria, and since September 2013, he has been working as a senior lecturer and research team member in the LMER laboratory at the department of electrical engineering, university of Bejaia, Algeria. His research area includes active power filtering, FACTs and power system.

Hocine AMIMEUR was born in Bejaia, Algeria on September 17, 1977. He received the engineer diploma in electrical engineering from the University of Bejaia in 2005. In 2008 and 2012, he received the M.Sc. and the Ph.D. degrees respectively from the University of Batna, Algeria. Since February 2011, he has been working as a senior lecturer and a research team member in the LMER laboratory at the department of electrical engineering, university of Bejaia, Algeria. His research area includes electric machine control, renewable energies and FACTs.