Low-voltage Power Supply Subsystem for a Sub-Orbital Particle Physic Instrument

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Abstract. *The Japanese Experiment Module–Extreme Universe Space Observatory (JEM-EUSO) is a wide-field (+/− 30° of aperture) 2.5 m refractor telescope to be installed in the International Space Station (ISS). The instrument looks downward from its orbit, into Earth's atmosphere, with the main objective of observing ultra-violet (UV) fluorescence light generated by Ultra-High Energy Cosmic Rays (UHECR) extensive air showers (EAS). It is a frontier particle-physics experiment, the first of its kind. The validation of the technical readiness level of such a complex and unique instrument requires prototypes at several levels of integration. At the highest level, the EUSO-Balloon instrument has been conceived, through French space agency (CNES). At a smaller scale and in suborbital flight, EUSO-Balloon integrates all the sub-systems of the full space JEM-EUSO telescope, allowing end-to-end testing of hardware and interfaces, and to probing the global detection chain and strategy, while improving at the same time our knowledge of atmospheric and terrestrial UV background. EUSO-Balloon will be flown by CNES for the first time from Timmins, Canada; on spring 2014.This article presents the low-voltage power supply (LVPS) subsystem development for the EUSO-Balloon instrument. This LVPS is the fully operational prototype for the space instrument JEM-EUSO. Besides design and construction, all performance tests and integration results with the other involved subsystems are shown.*

Keywords

DC-DC converter, power supply, stratospheric balloon, thermal-vacuum test.

1. Introduction

JEM-EUSO consists of a large telescope with a wide field-of-view, to be mounted on the ISS. It is the first space mission to explore the universe at extreme energies through the detection of UHECR impinging the Earth's atmosphere. Such interactions produce an EAS, a huge numbers of charged particles, mainly electrons and positrons, travelling through the atmosphere along the original direction of the incoming UHECR. They excite the atmospheric N_2, which immediately decays by fluorescence producing UV photons with wavelengths between 300 and 400 nm. Furthermore, the electrons and positrons are super-luminal inside the atmosphere and, therefore, also produce UV Cherenkov radiation. Both radiations are observed by JEM-EUSO from orbit at 400 km of height. Since electrons and positrons travel all at roughly the same speed, essentially that of light the net effect is that, from the point of view of the telescope, an EAS is observed as a light spot moving at the speed of light, thus defining a track on its focal surface. It is worth noticing that the Cherenkov photons are emitted along the propagation direction of the particles in the EAS, i.e., downwards. Therefore, those photons are only observed because of scattering in the atmosphere or after diffuse reflection on the top of optically thick clouds or on the ground. The latter produces a strong Cherenkov mark signaling the impact point of the EAS and it is extremely important for data reconstruction [1].

Although theoretically sound, the observational principle has never been tested from space. There are also considerable uncertainties with regard to the intensity of the Earth up-going UV background produced by the atmosphere and the ground due to both, the Moon and terrestrial sources, as well as the UV diffuse reflectivity of different types of ground (sand, snow, ice, clouds, vegetation, oceans, etc.) which can affect the reconstruction efficiency and the effective duty cycle of

the instrument. In addition to instrument complexity, an EAS has never been observed yet from space. Thus, a large scale comprehensive prototype is mandatory: EUSO-Balloon is such prototype.

EUSO-Balloon had being design and built by a consortium which, under the umbrella of CNES, includes laboratories from France, Germany, Italy, Japan, Mexico, Poland, South Korea and Spain. The instrument is a reduced version of JEM-EUSO which still comprises all the subsystems of the JEM-EUSO main mission. The instrument will operate at an altitude of 40 km during the night and measure photons in the UV range with a time resolution of 2.5 μs with a field of view (FOV) of the optics 12°× 12° (squared) and a large dynamic range. EUSO-Balloon also has the potential to detect for the first time a cosmic ray atmospheric shower from above, marking a key milestone in the development of UHECR science, and paving the way for any future large scale, space-based UHECR observatory, including of course JEM-EUSO [2].

Regardless of the payload, the power supply system is a key component. The Electrical Power System (EPS) of a spacecraft comprises power conversion, energy storage, regulation, power conditioning, overvoltage (OVP) and over-current (OCP) protections, and power distribution to the various users via the on-board (OB) LVPS [3]. These stages are generally divided into three sections: *the primary energy source*, which converts a fuel into electricity power. The *secondary energy source* for storage and regulation of energy and subsequently delivers electrical power to spacecraft and its payload. And finally, the *power control and distribution* network that is required to deliver appropriate voltage-current levels to all spacecraft loads when required [4].

The present work describes the LVPS developed for the EUSO-Balloon instrument. The paper is organized as follows: Section 2 gives a general description of the instrument; Section 3 presents the power distribution architecture; Section 4 details the LVPS requirements; Section 5 gives the specification subsystems; Section 6 describes the several modules that conform the subsystem; Section 7 summarizes several design considerations and Section 8 presents the various tests that were applied for the characterization of the system and validation of the compliance to its requirements.

2. EUSO-Balloon Instrument

EUSO-Balloon instrument consists, firstly, of a Fresnel optic array comprised by tree polymethyl-methacrylate (PMMA) square lenses for UV transmitting. After that, a focal plane detector composed of 36 multi-anode photomultiplier tubes (MAPMTs) with 64 pixels each representing 2.304 pixels, called photo-detector module (PDM). A 2°× 2° MAPMTs array, called elementary cell (EC), has its associated application-specific integrated circuit (ASIC), high voltage supply (HV) and HV switches. The 15°×15° cm PDM and the 100 cm × 100 cm Fresnel lenses provide a field of view of ±6 deg and shall observe in "nadir mode" that can be varied, in principle, during later flights in a range between 0° to 30°. A schematic description of the instrument is shown in Fig. 1.

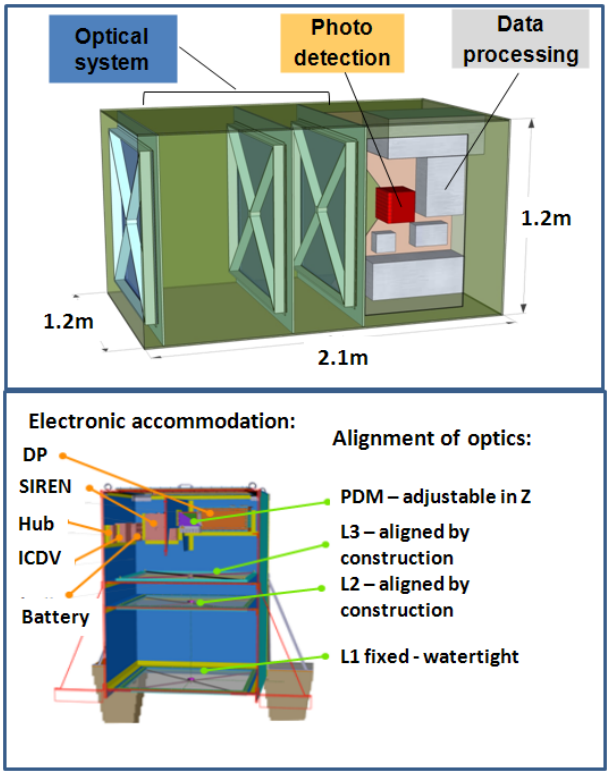

Fig. 1: EUSO-Balloon instrument description.

Therefore, the UV light entering in optics system is imaged on the PDM. The later normally works in single-photoelectron mode; however it can also extend its dynamic range in order to observe intense light signals thanks to the implementation of gain switches. The signal from each MAPMT is processed by the Front-End Electronics (based on the ASIC) and preliminary processed in the so-called PDM board, which is within the PDM structure where the first-level trigger is performed. Data are then transferred to the Digital Processor (DP) component where the second level trigger is first applied by the cluster control board (CCB), after that data are prepared to be sent as a part of telemetry information. Data management and storage, instrument control and commanding are managed by components within the DP structure. As shown in Fig. 2, the main subsystems of the EUSO-Balloon instrument are: telescope (TES), electronic (ELS), power (PWS), and the camera (CAM), [2].

As can be observed in the block diagram of the instrument in Fig. 2, the tree main components of PDM structure are: EC, high-voltage power supply (HVPS), and PDM board (PDMB). The cores of these components are based on ASICs and field programmable gate arrays (FPGAs) in order to perform signal acquisition and digitalization as a part of first trigger level detection. The DP structure comprises the CPU, data storage (DST) hard disks, cluster control board (CCB), clock board (CLKB) which dictates the system master clock, GPS receiver (GPSR), and the housekeeping (HK). The latter monitors the instrument; generate alarms, reset signals and powers on/off every other subsystem at the request of either the CPU or ground. As in the PDM structure, the cores of all these components are FPGAs and microprocessors unit (µPU) which have tight constraints about voltages levels requirements. As a first approximation, one LVPS module has been considered for each structure: LVPS-PDM and LVPS-DP.

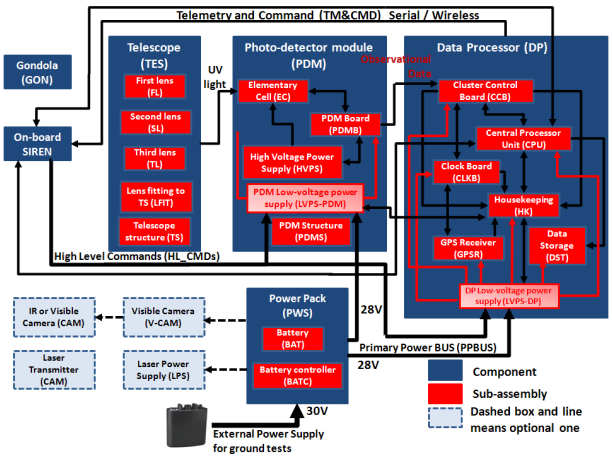

Fig. 2: EUSO-Balloon block diagram.

3. Power Distribution Architecture

The latest high-performance FPGAs, ASIC's and µPU require increased high performance on voltage levels from power supply. Typical requirements include low voltages (sometimes less than 1 V), high currents (up to 3 A), tight regulation (less than 1 %), fast transient response, and even supply voltage sequencing.

In space and near-space environment, it is recommended [3] that buses voltage should not be selected below 20 Vdc and not to exceed 125 Vdc. Bus voltages below 20 Vdc might lead to unwieldy current densities, while bus voltage above 125 Vdc might easily generate dangerous potential gradients, leading to ionization of air molecules (plasma), causing coronal and electric arc discharges, in particular during tests in partially pressurized environments. A 28 V power bus is often used as internal power bus in satellites, aircrafts and vehicles under specific military standards or program requirements [5]. It also has to be considered that the biggest selection of components of-the-shelf (COTS) is available for operating voltages between 28 Vdc and 50 Vdc [3].

Many issues play an important role in determining the best power distribution architecture, e.g., the kind of loads, the circuitry dimensions, the amount of current and low output voltage values, thermal management, transient response, etc. The latter produces lack of scalability and puts small configurations at cost disadvantage [6]. Therefore, a detailed analysis and a trade-off study must be performed in to ensure the most appropriate selection of power distribution architecture to meet the specific mission requirements [7]. For that purpose, a system design criteria must be stated considering factors like cost, low profile, system efficiency, dynamic response, reliability, availability of components, heat distribution, redundancy and development schedule. These factors help not only in selecting the most appropriate power distribution architecture, but will also constitute a basis for selecting the most appropriate power technology.

The DC-DC converter unit (DDCU) is a power device that typically receives power from a main power bus and regulates their outputs to a narrow voltage range. As already mentioned, the satellite power bus voltage can range from 20 Vdc to 120 Vdc. Meanwhile, payload electronic and bus system typically require 3.3 Vdc to 28 Vdc, although at present the voltage requirements are decreasing towards 1 Vdc and less for digital loads [8]. Taking into account the high cost of these type of missions and the impossibility of repairs, the DDCU must rigorously comply with general requirements as reliability tests, good efficiency (above 80 %), good load and line regulation, low output ripple, electromagnetic compatibility (EMC) standards and input/output (I/O) protections.

Due to the instrument hierarchical disposition and number of components, see Fig. 2, four LVPS modules were proposed, developed and housed inside the DP structure. The LVPS represent a transformation and isolation stage between PWS and payload. Meanwhile, final transformation and tight regulation are met by implementing non-isolated Points of Load (niPOL) converters or linear regulators (LRgs) OB of each individual subsystem, as shown in Fig. 3. The increased number of LVPS modules has the undeniable disadvantage of pushing up costs; nevertheless, it improves heat dissipation, system reliability, while decreasing electromagnetic interference (EMI) contamination by ground loops generated because of ground planes sharing of different voltage levels subsystems.

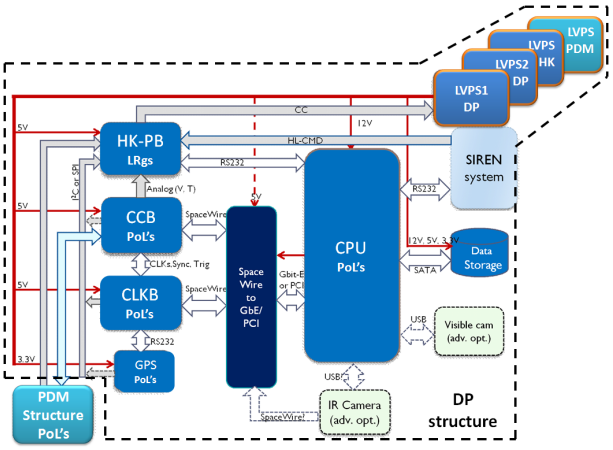

Fig. 3: EUSO-Balloon power distribution architecture inside of DP structure.

Additionally, in order to avoid radiated and conducted EMI, generated by DDCU within the PDM detector structure, which in principle has the most EMI-susceptible components, it was decided to install the LVPS module of PDM subsystem (LVPS-PDM) inside of the DP rack, see Fig. 3. Additionally, the part of LVPS devoted to the DP components was distributed into three modules, according to importance and criticality of the respective components to instrument performance. This strategy also facilitates heat dissipation and increases the overall reliability of the instrument. The three modules are: LVPS-HK, which powers the monitoring subsystem, HK; LVPS1-DP powering CCB, responsible for the second level trigger process, CLKB, the clock board, and the GPS receiver (GPSR); and LVPS2-DP which powers both the CPU and the data storage subsystem (DST) comprised by two 1 TB solid state disks.

4. LVPS Requirements

The LVPS subsystem must distribute power in a reliable way to each one of the other subsystems of the EUSO-Balloon instrument, while complying with the various specification requirements of those subsystems. Those requirements are, in fact, the input data of the design stage. We group the requirements in 3 broad categories listed below: functional, environmental and of communication.

4.1. Functional Requirements

- The LVPS shall supply power in a reliable way to PDM and DP structures.
- The LVPS subsystem shall consist, at least, of two different power distribution modules: LVPS-PDM and LVPS-DP.
- The LVPS modules shall provide isolation interface between 28 V bus of PWS and all payload subsystems.
- The isolation stage will comprise isolated DDCU with efficiencies equal or higher than 80 %.
- The LVPS modules shall withstand a lower voltage level, as input, from battery power pack (PWP).
- The regulation stage shall be performed directly at load (as close as possible) for best performance.
- Tight regulation stage will comprise niPOL converters with efficiencies higher than 90 %.
- Propagation failures inside of LVPS modules should be controlled. If any failure event occurs, it cannot be propagated to either the primary or secondary sides of the isolation stage.
- The LVPS modules shall provide remote on/off functionality, in order to be controlled from OBSIREN.
- The DDCU shall provide wide input voltage range in order to withstand input voltage oscillations.
- The DDCU shall provide input circuit protection function in order to protect circuitry attached to main bus by some abnormalities.
- The DDCU shall provide output over current protection function.
- Input and Output EMI filters should be considered in the design of the LVPS modules.
- The maximum PCB dimensions shall conform to the 3U Eurocard size board standard [19].
- The weight of LVPS subsystem must not exceed the 5 kg.

4.2. Environmental Requirements

- The LVPS elements must withstand temperature variations in the range $-20\,^{\circ}\mathrm{C}$ to $+50\,^{\circ}\mathrm{C}$ during operation.
- The LVPS elements must accept a storage temperature $> -40\,^{\circ}\mathrm{C}$.
- The LVPS elements must withstand shock acceleration levels of at least 3 G.
- The LVPS elements must be able to operate at very low atmospheric density, 3 mbar of pressure.

4.3. Communication Requirements

- Tele-command (TC) shall be used for turning on/off remotely LVPS modules.
- Status on/off by contact closure (CC) signal shall be provided from LVPS modules.
- Telemetry (TM) data, about voltage and current (V&I) levels, shall be generated and transmitted from LVPS modules to the HK subsystem.

5. LVPS Specification Subsystems

The LVPS requirements stated in the previous section define, to some extent, the interaction level with other subsystems. On other hand, the specifications describe the technical subsystem features. This explicit information provides the procedure to be followed for determining whether the requirements are met [9]. Table 1 lists the subsystem specifications regarding the EUSO-Balloon block diagram shown in Fig. 2.

The PWP in Tab. 1 is the instrument power source during flight, and it provides a non regulated bus (NRB) nominally of 28 V with a power capability of 100 W. However, this NRB may drift down up to 18 V, due to the normal discharge of its battery cell array, during the flight. Those variations must be accommodated by the LVPS subsystem by a DDCU proper selection.

Moreover, as can be seen in the voltage column of Tab. 1, it is necessary to create an intermediate bus semi-regulated (SRB) between the isolation stage and tight regulation, in order not to decrease the overall efficiency of the first stage. However, a SRB value must be selected based on two aspects: the minimum and maximum output voltage of first stage (tolerance) and input voltage range of next stage (final transformation and tight regulation).

Commonly, supply power for digital logic and IC processing devices is done through linear regulators and niPOL converters, depending of load, which nominal input voltage is 5 V. At this value the output voltage is maintained, with efficiencies higher than 90 %, within a tight regulation band to ensure proper functionality of the devices [10]. Output voltage tolerances of 10 % in isolation stage are expected in order to comply with the input voltage range of payload.

6. LVPS Modules Description

As stated in section 3, Four LVPS modules were proposed: LVPS1-DP, LVPS2-DP, LVPS-PDM and LVPS-HK. As an example, Fig. 4 shows LVPS2-DP diagram description.

Each LVPS module has, at least, three header connections represented in Fig. 4 as DB connectors: input power, input/output (I/O) TM&TC connector and output power. An important goal of the present work was to propose the use of industrial isolated DDCU (denoted with DDCU1 and DDCU2) in order to keep costs as low as possible. However, this proposal carries a certain level of risk, since most DDCU are tested by the manufacturer only under operation condition at 2 km of height. For example, Tab. 2 shows the maximum operational conditions tests reported by TDK Lambda switching power supplies manufacturer.

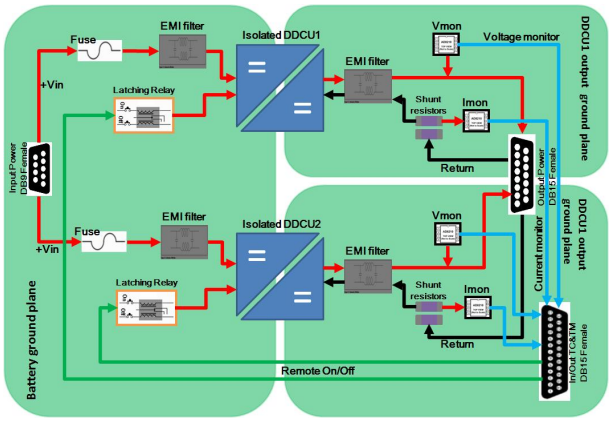

Fig. 4: LVPS2-DP diagram description.

In order to provide instrument flexibility and reliability, a remote On/Off function was implemented (green lines in Fig. 4) based on a power switch circuit and dual pole dual throw latching relay (DPDT-LR), the last showed in Fig. 4 orange framed. On other hand, LC and pi filters at I/O DDCU were implemented (denoted as EMI filters) in order to offer protection to conducted emissions interference sources of other equipments coming from cables and wires.

Also, from the point of view of flexibility and regarding future flights scheduled for EUSO-Balloon, fuses at each input converter were located for inrush energy and maximum dc input current protection. Furthermore, V&I monitoring circuits (labeled as Vmon and Imon on Fig. 4) were implemented in order to provide TM of LVPS performance subsystem. Finally, in order to keep isolation between main power bus and payload secondary side three different ground planes were planed during PCB design. The last helps avoiding ground loops and less contamination between subsystems.

Tab. 1: Subsystem specifications.

Subsystem	Component	Element Subsystem	Power (W)	Voltage (V)	Electronic
PWS	PWP	Battery	100	28	N/A
	PDM	EC	10	1.5	4 ASICs
				3.3	
		PDMB	10	1	1 FPGA
				1.5	
				1.8	
				2.5	
				3.3	
	DP	CCB	5	1.2	1 FPGA
				2.5	
				3.3	
		CLKB	4	1.8	1 FPGA
				2.5	
				3.3	
		DST	15	5	2 Hard Disks
		HKB	5.5	±12	1 MCU
				5	
			0.5	3.3	
		CPU	12	12	Intel Atom MPU
				5	
		GPSR	1.5	5	GPS module receiver

Tab. 2: TDK Lambda DDCU test operational conditions (based on MIL-STD-810F).

Test condition	Operating combined temperature/altitude		Non-operating combined temperature/altitude	
Temperature (°C)	0	40	−40	70
Altitude (km)	12.2	12.2	15.2	15.2
Test duration (hr)	2	2	6	6

7. LVPS Design Considerations

Is important to note that a power supply subsystem assumes a very important role within any system, it gives power in a consistent and reliable way to circuits system. Besides protects the system against electrical abnormalities like a transients and short circuits events. In a few words, if the supply experiences a failure within itself, it must fail gracefully and not allow the failure to reach the subsystems [11].

Following these considerations, and in order to produce a good design, many aspects must be considered prior to the beginning of the design process. In particular, the EUSO-Balloon instrument environmental operation condition at 40 km of altitude implies some constraints related to components selection, heat dissipation, EMC, grounding architecture, etc.

7.1. DDCU Selection

As new generations of programmable digital devices (FPGA's, DSP's, ASIC's, etc.) enter the market to meet the growing demand for increased bandwidth, and data processing speed OB subsystem instruments, these devices place unprecedented constraints in power supplies (PS). Low voltage supply and high operating current are the main features required from new digital devices.

Correspondingly, a detailed analysis and a trade-off study must be performed to ensure that the specific mission requirements are met [7]. For that purpose, design criteria factors, such as cost, low-profile, electrical performance (input voltage range, load and line regulation, efficiency, tolerances, etc.), availability (procurement times), heat distribution and EMC were considered.

Based on the above considerations, isolated DDCU from three different manufacturers (TDK Lambda, Tracopower-TPW and XPPower-XPP) were selected. The DDCU main features are summarized in Tab. 3 according to each LVPS module. As can be observed in Tab. 3, LVPS1-DP which is devoted to CCB, CLKB and GPSR subsystems creates a 5 V secondary bus voltage, as LVPS-PDM does, with the main aim of providing a better regulation for FPGA by implementing niPOL converter OB in each subsystem.

Meanwhile LVPS2-DP and LVPS-HK, create a 12 V secondary bus voltage in order to power linear regulators, which supply 5 V level for the microprocessor unit (MPU) and microcontroller unit (MCU), respectively. 5 V and 3.3 V were also generated separately for not critical components (gates, drivers, etc.).

7.2. Electromagnetic Compatibility

EMC is the ability of electrical or electronic equipment to function in the intended operating electromagnetic environment without causing or experiencing performance degradation due to intentional EMI [12]. In order to achieve EMC, the influence of electrical noise in a system must be minimized. Therefore, it is necessary to establish an EMC design flow diagram based on three parallel branches: mechanical design, electrical design and system design as is showed in Fig. 5, [13].

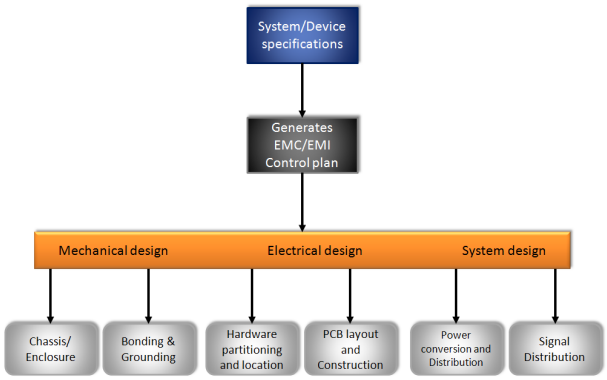

Fig. 5: EMC design flow diagram.

Since switching mode power supplies (SMPS) have high voltage and high current switching waveforms that generate EMI, in both conducted and radiated emissions, enclosure and grounding become a very important issue [14].

Therefore, in order to minimize radiated emissions, LVPS modules were housed inside 19" plug-in units which serve as accommodation up to two PCB. The mechanical dimensions comply with the IEC-60297-3-102/IEEE 1101.1/11 standard. Figure 6, shows the LVPS modules frame type plug-in unit enclosure. This plug-in units match 3U eurocard standard [19], and also includes a conductive foam EMI gasket consisting of a polyester textile yarn uniformly platted which provides high shielding performance (60–100 dB), high level of flame resistance (UL94-V0), mounted using pressure sensitive adhesive (PSA) and is able to operate at higher frequencies due to no gaps on their construction.

Additionally, these plug-in cabinets are fitted into metal chassis DP rack box that serves as a shield for all the subsystems housed inside it. Figure 7 shows the DP box (rack) with most of the sub-systems installed and labeled.

Therefore, the fields from all the radiating surfaces are shielded, with noise coming only from cables or wires that enters/exit holes and slots made in the box. In order to achieve this, the shield must be a good conduction plate with the least possible number of me-

Tab. 3: Main specifications of DDCU.

Parametr	**LVPS1-DP**		**LVPS_PDM**	**LVPS2-DP**		**LVPS-HK**	
Mfgr/DDCU s qty	TDK (1)	TPW (2)	TPW (2)	TPW (1)	XPP (1)	XPP (2)	
Subsystem	CCB	CLKB and GPRS	FPGA and EC-ASIC	CPU	DST	HK-MCU and HK_LVDS	
Input voltage range (V)	18 to 36			9 to 36			
Output power (W) with safety factor	6	5 and 2 (respec)	15 (each one)	15	30	8	2
Output voltage (V) secondary bus voltage	5		5.5	12	5	±12	3.3
Line and load regulation (%)	0.2–1		0.2–0.3	0.2–0.5		0.2–0.5	
Efficiency (%) at full load	80–82		84	87–91		80–86	
Operating temperature ranges (°C)	−40 to 85					−40 to 100	
EMC	Safety stds: UL60950-1 IEC60950-1 EN60950-1 Conducted noise: EN55022 Class A nad B, FCC part 15			Safety stds: UL60950-1 IEC60950-1 EN60950-1 Conducted noise: EN55022 Class A and B, FCC part 15 ESD Radiated and conducted immunity: EN61000-4-2, 4-3, 4-6 respectively			
Vibration	MIL-STD-810F 10–55 Hz, 2G, 30 min along X, Y			MIL-STD-810F		—	

Tab. 4: Load regulation of LVPS modules.

Module	**DDCU subsystem**	**Secondary bus voltage (V)**	**%LdReg @Vin_{nom}**	**%LdReg @Vin_{low}**
LVPS1-DP	CCB	5	1.4	1
	CLKB	5	1.2	1
	GPRS	5	2.8	2.6
LVPS2-DP	CPU	12	0.17	0.25
	DST	5	0.74	0.96
LVPS-PDM	FPGA	5	1.36	1.31
	EC-ASIC	5	1.35	1.32
LVPS-HK	Arduino MCU	±12	7.3	7.4
	LVDS	3.3	10	7.96

chanical breaks and lower impedances between the current sources and the ground reference point (GRP).

The GRP at the EUSO-Balloon instrument is based on a single point grounding topology, with star connection tying all subsystem together, throughout the LVPS modules and up to the negative borne of the battery, which is called mechanical ground (GND_M), see Fig. 8.

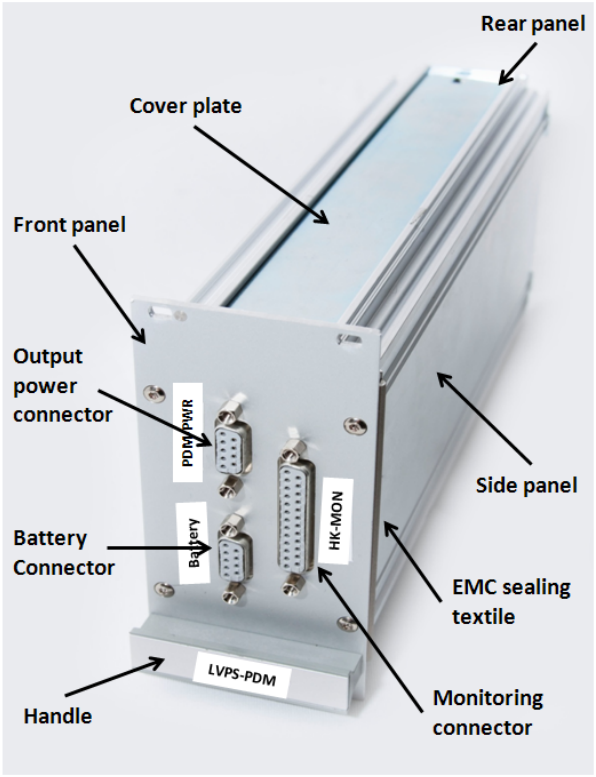

Fig. 6: 3U plug-in unit of LVPS-PDM module (100 mm × 227 mm × 61 mm).

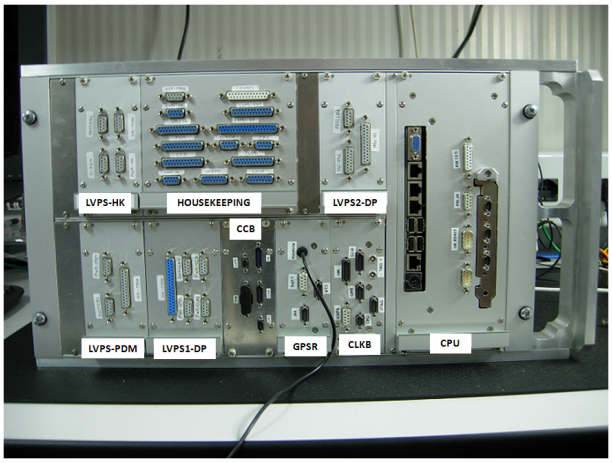

Fig. 7: DP box with all subsystems fitted (220 mm × 235 mm × 498 mm).

This topology requires a considerable number of conductors, which is generally not practical in large distributed subsystems [15]. On other hand, this architecture accomplishes the functions of signal return, while helping to control common-impedance interference coupled between subsystems. Additionally, to avoid closed-loop paths for noise current contamination, separately ground planes were implemented for each LVPS module (see Fig. 8) at secondary side output (right winding transformer) of magnetic isolation transformer. These ground planes are denoted in Fig. 8 with small squares per each winding output transformer. On other hand, most of DDCU were selected built-in metal enclosure in order to decrease radiated interference, as well as, be less susceptible to EMI. Cables were implemented as a twisted pair and connectors provided with back-shielding in order to minimize EMI radiation.

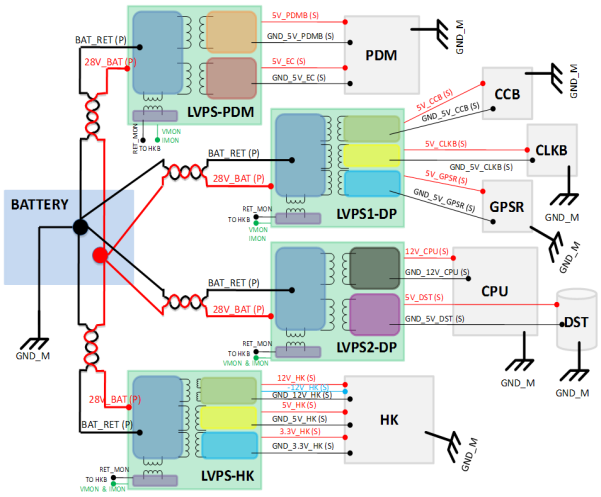

Fig. 8: EUSO-Balloon grounding architecture.

7.3. Thermal Management

Due to the lack of natural convection and reduced air heat conductivity in heat dissipation issue, some specific techniques must be implemented to conduct the heat generated by DDCU on different subsystems to the external structure for dissipation.

LVPS subsystem contains semiconductor devices, capacitors and other components that are vulnerable to thermal stress. In this particular case, the power devices inside of DDCU modules represent the major heat source. Therefore, an adequate thermal architecture becomes vital to limit the DDCU temperature to a lower value for extremely high reliability performance. As an example, Fig. 9 shows in a schematic description the thermal parameters involved on a DDCU mounted in two layers PCB. Parameters denoted with θ are described as thermal impedance of some heat power dissipation path. In that way, θ_{JA} represent thermal impedance from the junction, internally of DDCU un-

der test, to the ambient environment and can be expressed as Eq. (1) shows:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}. \tag{1}$$

There are two primary heat paths for the DDCU in Fig. 9, represented by their associated thermal resistance. The first path travels from the junction of DDCU to the plastic molding at the top of the case, θ_{JC}, and then to the ambient air, θ_{CA}. The second path is from the junction of the DDCU to an exposed pad, θ_{JEP}, when it exists. Therefore, the exposed pad is connected to the PCB, where the heat travels through the surface and finally to the ambient air [16]. Following the same path, θ_{Cu} represent the thermal resistance of our board's cooper to lateral heat transfer. Meanwhile, θ_{FR4} is the thermal resistance between the cooper planes provided by the vertical resistance of FR4 laminate, and θ_{SA}, represent the thermal resistance from the surface of the PCB to the ambient air.

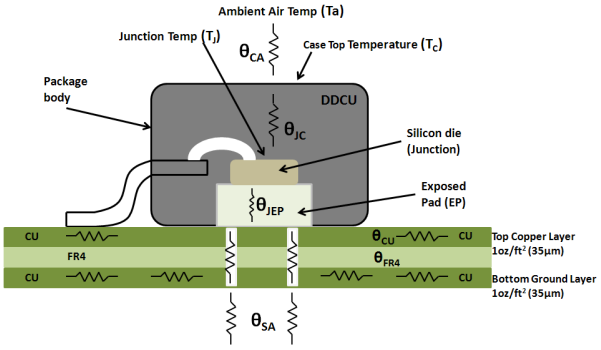

Fig. 9: DDCU thermal resistance model for a two layers PCB.

Therefore and concerning in our case. The most critical module, because of power consumption and transient response conditions, is the DDCU parallel arrangement for DST section of LVPS2-DP. For this arrangement the heat transfer path is through the case to ambient air.

Furthermore, special attention is needed in order not to exceed $\sim$ 105 °C case temperature for a reliable operation, otherwise thermal protection is activated. Taking into account this issue, a preliminary setup under ambient temperature and normal pressure conditions, was proposed in order to get a better knowledge about how long does it take reach this critical temperature. As a first result, 20 min (at 5 A) were necessary for reaching $\sim$ 85 °C with a positive slope in the curve obtained. Therefore, it is necessary to implement heat dissipation architecture, according to our case, to maintain the temperature bellow critical level. This thermal architecture is based on conduction method using a heatsink (HS) as interface material between DDCU of LVPS2-DP and DP rack structure.

Regarding this issue and the thermal background above described, now θ_{JA} is actually made up of at least two separate thermal resistances in series. One is the thermal resistance inside the device package, θ_{JC}, and the other one is the resistance between the case and the ambient, θ_{CA}. The last term can be splitted into θ_{CS} and θ_{SA}, thermal resistance from case to HS and thermal resistance from HS to ambient respectively [17] resulting in Eq. (3):

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}. \tag{2}$$

However, in order to select a HS the term θ_{SA} has to be calculated. Therefore, assuming the next safety conditions and specification from DDCU datasheet: T_{Jmax} = 100 °C, T_{JAmax} = 50 °C, T_{Cmax} = 90 °C, P_D = 7 W and, using Eq. (1), Eq. (3) and Eq. (4), θ_{SA}term can be obtained by Eq. (5):

$$\theta_{JC} = \frac{T_{Jmax} - T_{Cmax}}{P_D}, \tag{3}$$

$$\theta_{CS} = \frac{t}{k \cdot A_C}, \tag{4}$$

where t is the thickness material (9.6×10^{-3} m^2), k is the thermal conductivity of aluminum 3003-O (190 W/m·°C), and Ac is the contact area between DDCU and the HS (1.3×10^{-3} m^2):

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{SC}). \tag{5}$$

Consequently, a θ_{SA} = 5.68 °C/W was obtained which implies a selection of HS rated at 5.68 °C/W, or less. Therefore, and regarding the plug-in unit box in Fig. 6, the thermal architecture and its components showed in Fig. 10 were developed.

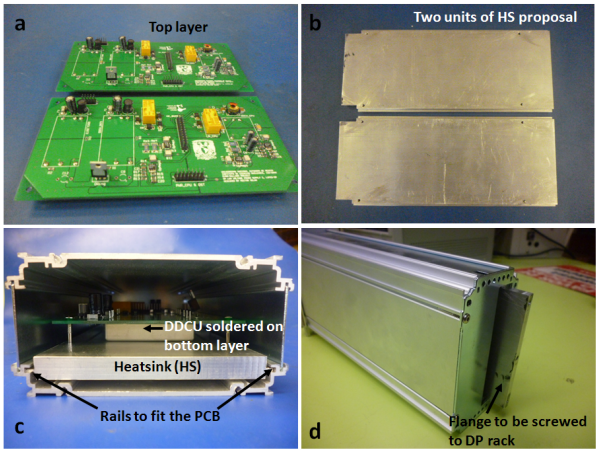

Fig. 10: (a) LVPS2-DP PCB, (b) Heatsink proposed, (c) PCB, heatsink and unit box assembly, (d) Heatsink rear side to be assembly with cooling plate of DP structure.

As can be seen in Fig. 10(a), most of elements are in the top layer while the converters are in the bottom layer, unlike the rest of the power modules PCB

in which all the components are in the top layer. Consequently, the converters make direct contact with HS surface (as is showed in Fig. 10(b)) conducting the heat to HS edge coming out across the rear side panel of plug-in box, as can be seen in Fig. 10(d). Finally,the HS edge (rear side) has holes in order to be screwed to DP rack cooling metal backplane, if it is necessary. This metal backplane is connected to heat metal conductive bars, and then connected to external structure of balloon gondola improving in that way the thermal management of all instrument.

8. Tests

In order to qualify the LVPS subsystem performance under the balloon environmental conditions, two sorts of tests were done. The first one was devoted to evaluate the electrical performance of LVPS modules under different load ranges (10 % to 100 % of full load) considering worst case (WC) scenario. The second one was focused in evaluating the critical electrical performance levels (at full load) under approximate vacuum environment (∼3 mbar) applying temperatures variations, during the test, of −20 °C to 55 °C.

8.1. Electrical Performance

The aim of this test is to characterize the four LVPS modules according to each subsystem specifications. A dc electronic load (dcEL) simulator, specifically developed at our group for this purpose, was used in order to automate the test process. The main idea of this dcEL is based on the use of a simple feedback loop to allow the transistor work as a current drain in current regulation mode, or as well as a voltage source in voltage regulation mode [18]. At this particular case, current regulation mode is used for characterizing voltage sources, in which the power source must deliver a specific current level setting by serial software interface to dcEL hardware. Figure 11 shows the electrical performance setup used to perform this test.

Basically, the setup above consists of a main laboratory power supply (LPS) labeled as 1, which provides the 28 V primary power bus voltage to the LVPS modules at number 2. Inside of LVPS modules, DDCU isolate and transform to a secondary power bus voltage depending on each subsystem. On other hand, dcEL at 3 receives commands from HK subsystem labeled as 4, powered with an auxiliary power source at number 6. HK communicates with a PC software interface, showed at 5 via, serial port. The software fixes the current level that should provided LVPS module to dcEL. At same time LVPS module provide V&I levels as TM

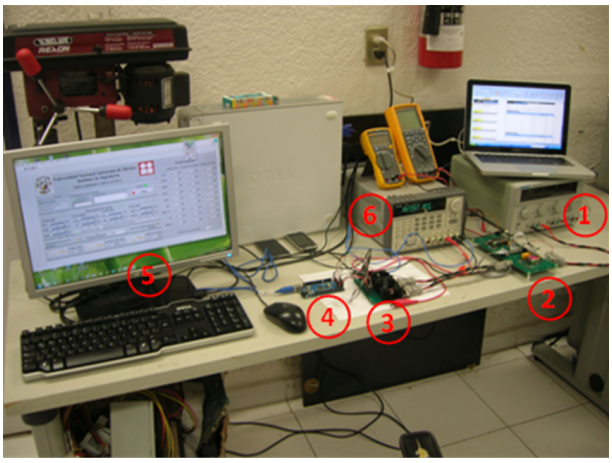

Fig. 11: Electrical performance set-up: main power (1), LVPS module (2), DC electronic load (3), HK subsystem (4), PC software (5), andauxiliary power supply (6).

information about DDCU status consumption to HK subsystem.

Therefore, based on setup explanation above, parameters like load and line regulation (LdReg & LnReg) were obtained at each LVPS module output connector using Eq. (6) and Eq. (7), [11]. Table 4 shows load regulation values for each LVPS module sections. Performance curves related to efficiency vs output current and input voltage (LnReg) also were obtained. Figure 12, Fig. 13, Fig. 14 and Fig. 15 show the line regulation according to voltage level provided by LVPS modules to each subsystem.

$$\%Load_{\mathrm{REg}} = \\ = \left(\frac{V_{OUT_{Full\_load}} - V_{OUT_{10\%\_load}}}{V_{OUT_{50\%\_load}}} \right) \cdot 100, \qquad (6)$$

$$\%Line_{\mathrm{REg}} = \\ = \left(\frac{V_{OUT_{High\_Vin}} - V_{OUT_{Low\_Vin}}}{V_{OUT_{Nom\_Vin}}} \right) \cdot 100. \qquad (7)$$

The percentage of LdReg indicates the variation in the output voltage in response to a change in load current, and is a reference to LVPS subsystem in order to comply with the output voltage tolerances. Load regulation percentage measurements were made varying the load from 10 % to full load in both cases, with nominal input voltage (28 V) and low input voltage (18 V) which is WC condition level.

Figure 12, Fig. 13, Fig. 14 and Fig. 15 shows LnReg plots of subsystems powered from 5 V, 5.5 V, 12 V and 3.3 V secondary SRB respectively. Those curves shows output voltage variations less than 10 %, at 90 % of full load, which comply with the subsystem specification requirement. The behavior of curves is almost linear, a slightly increment (less than 10 mV) at the

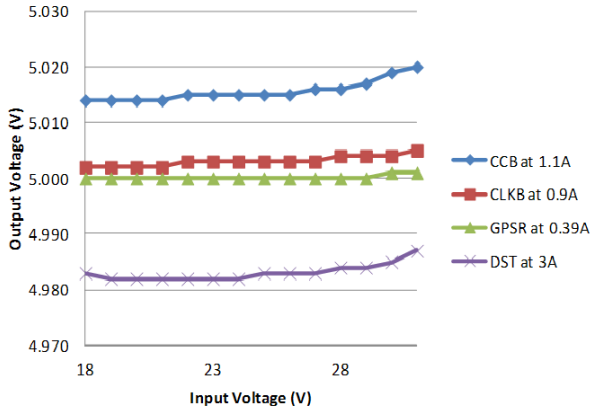

Fig. 12: Line regulation of subsystems powered with 5 V.

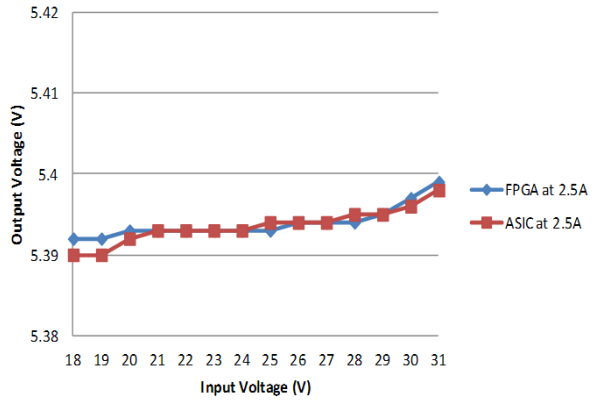

Fig. 13: Line regulation of LVPS-PDM subsystems powered with 5.5 V.

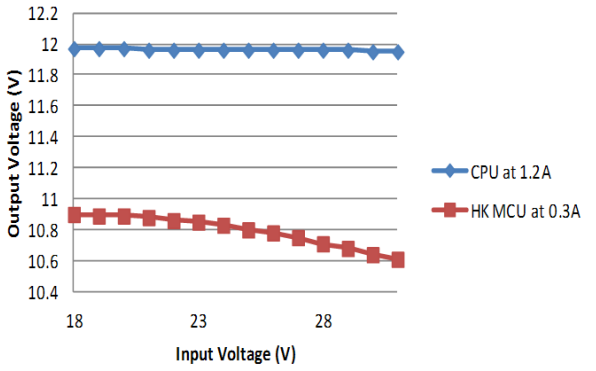

Fig. 14: Line regulation of subsystems powered with 12 V.

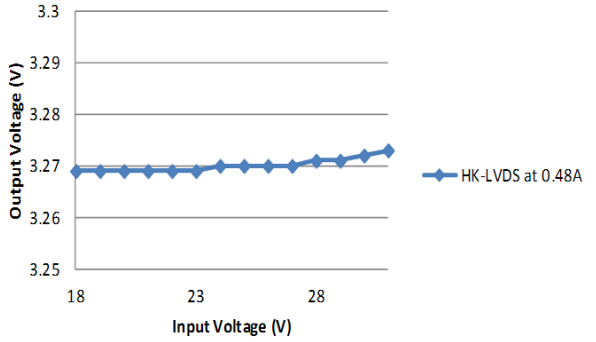

Fig. 15: Line regulation of subsystems powered with 3.3 V

end of curves ($Vin > 28$ V) is due to the temperature increase in resistors loads which cause increasing resistance value and consequently decreasing in current level demand which is compensated increasing the output voltage in order to keep a constant output power.

The LnReg term represent the change in output voltage in response to a change in the input voltage; these tests were planned considering the possible voltage range provided by PWP (battery), which goes from 18 V to 30 V. Besides, it is important to note that the DDCU input voltage range fits perfectly with variations range from battery.

On other hand, in Fig. 14 it can be observed a voltage drop in HK curve from 12 V to less than 11 V at 18 V input voltage on "x" axe. Figure 14 shows, at 24 V, a voltage drop that exceeds the 10 % specified. This abnormality is due to bad LdReg DDCU value obtained in Tab. 4. However, this abnormality is acceptable and compensated by the input voltage range of linear regulator in HK arduino board, from 7 V to 15 V. Voltage drop due to resistance cables represents a critical issue in any power distribution system. For this particular case, 0.5 m cables length with resistance of 0.15 Ω including connectors at the end were used. The latter do not represent a significant voltage drop at most cases. Moreover, efficiency curves of each LVPS modules were obtained, according to each subsystem demand. The test consisted in varying output current demanded with increment of 10 % steps of full load.

The last was done under WC condition ($Vin = 18$ V) in order to observe the behavior of each LVPS subsystem at maximum current levels. Therefore, in order to have a better appreciation of efficiency behavior on each case, Fig. 16 combines efficiency curves of those subsystems which current consumption is about 3 A, Fig. 17 groups subsystems which current consumption is about 1.2 A; meanwhile Fig. 18 shows those subsystem which demand is about 0.5 A.

The curves describe how efficiency improves meanwhile full load consumption is reached. However, is important to note that the maximum efficiency obtained in curves (from 60 % to 87 %) do not match with the converters efficiency, at full load, which are higher. The last is because of test measurements includes PCB parameters as impedance traces, planes, components, connectors, etc.

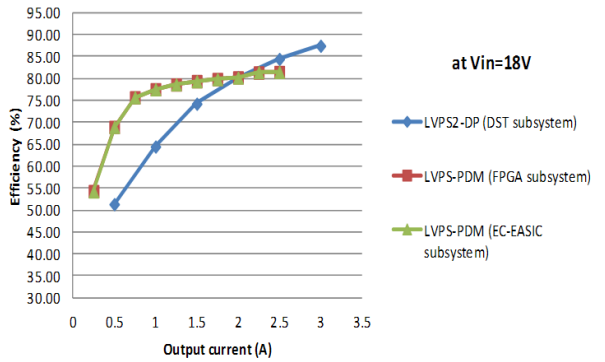

Fig. 16: Efficiency curves subsystems of approximately 3 A current consumption.

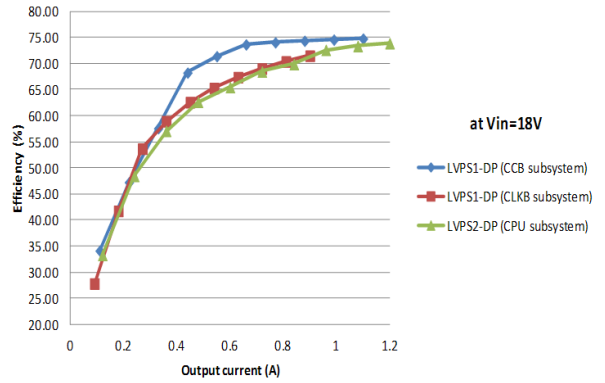

Fig. 17: Efficiency curves subsystems of approximately 1.2 A current consumption.

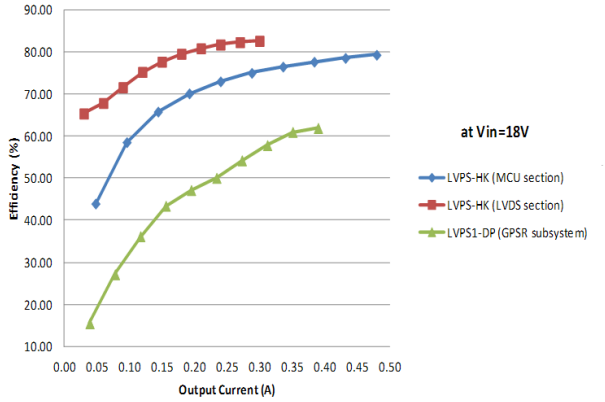

Fig. 18: Efficiency curves subsystems of approximately 0.5 A current consumption.

1) Turning On/Off LVPS Modules

In order to test the reliability of each module of power distribution system, and at the same time the interaction with HK (also designed and provided by our group) the setup showed in Fig. 19 was implemented.

Commands provided by an external PC were sent to HK subsystem. The commands were interpreted and executed by HK; which sends two high level commands (HL_CMD's) to LR's located OB LVPS modules. A HL_CMD is represented by a 9 V to 15 V amplitude of 10 ms pulse width. These commands are used in order to bias the internal coils of LR's, and diodes were included in design for feedback current protection.

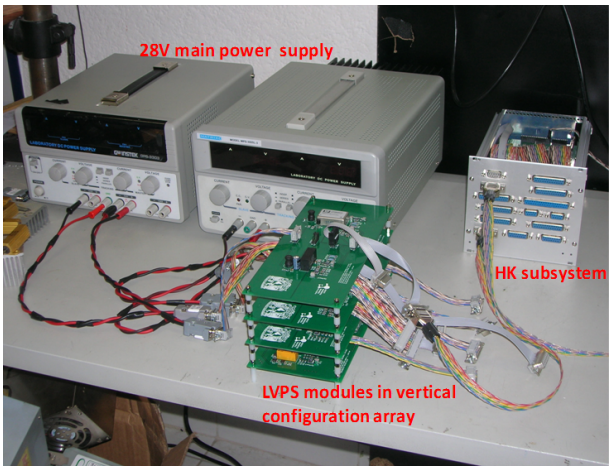

Fig. 19: Set-up for turning on/off LVPS modules.

In order to minimize the test space required, LVPS modules were arranged in a vertical assembled configuration as can be observed in Fig. 19. Finally, two dual laboratory power sources were added to the test setup in order to provide the 28 V primary bus voltage. This more complex setup was used to verify the four LVPS modules power consumption (without load) at the moment of turning-on, and the TM information of current consumption levels from current monitoring circuits at the LVPS modules. Also, a mechanical assembly was done in order to improve reliability during the testing process.

Table 5 shows the power consumption of LVPS modules (without load) after a successful turning on/off process, and monitored voltage levels obtained from voltage monitoring circuit as TM information. The voltage monitoring circuit is based on a non-inverter amplifier, with a constant gain factor of 0.326. In that way, a 3.3 V level correspond to 1.07 V, 5 V level correspond to 1.63 V, meanwhile 12 V level correspond 3.9 V output voltage.

Related to current monitoring and due to maximum current consumption subsystem (∼4 A), it was decided to use a shunt resistor as input of circuit based on OpAmp which relationship of output voltage level and current consumption is 1:1. Therefore, TM information levels obtained are presented in section 8.3.

Tab. 5: Load regulation of LVPS modules.

Subsystem	Secondary voltage by LVPS (V)	Consumption without load (A)	Monitored voltage (V)
CCB	5	0.03	1.613
CLKB	5	0.005	1.688
GPRS	5	0.02	1.678
PDM FPGA	5.5	0.025	1.716
PMD EC-ASIC	5.5	0.025	1.707
CPU	12	0.07	3.677
DST	5	0.1	1.6
HK-MCU	± 12	0.015	3.735
HK-LVDS	3.3	0.01	0.914

2) Mechanical Assembly of LVPS Modules

As mentioned in section 7.2, plug-in unit boxes were used for enclosing each LVPS module. Figure 20 shows the final mechanical assembly of LVPS modules.

Fig. 20: Mechanical assembly of LVPS modules.

These mechanical boxes were housed into a provisional euro rack structure, together with the HK subsystem, in order to interconnect them in easier way. Then, we were ready to perform the thermo-vacuum tests.

8.2. Heat Dissipation

The suborbital environmental conditions limit heat dissipation to conduction and radiation. This, coupled with the very localized injection of heat at the electronic boards, makes of heat dissipation an important issue. In particular, in the case of the LVPS, the heat generated by the DDCU must be piped to the external mechanical structure. LVPS2-DP PCB, in particular, represents a critical case due to the power demand of its clients, which may reach up to ∼4 A for DST and 1.25 A for CPU.

Furthermore, this steady state consumption due to different CPU operation modes and to several hardisk accessing processes (read/write), many transient events were generated. These transients cause not only high peaks of current, but also demand a faster response from the DDCU. Such transients are difficult to characterize and, after several tests during the first integration phase of the LVPS with the DP unit at INFN-Naples, Italy, a PCB design based on two DDCU in parallel was proposed to deal with them.

In order to manage the increase heat production on the latter design, a HS was designed in order to improve the dissipation from three DDCU of LVPS2-DP module. The Fig. 21 shows the mechanical assembly between HS and LVPS2-DP PCB inside of module.

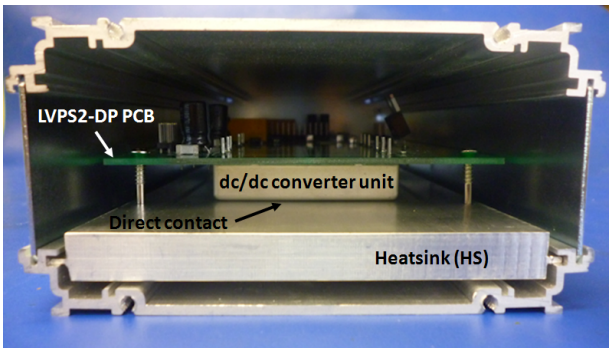

Fig. 21: Mechanical assembly between LVPS2-PCB and heatsink.

8.3. Thermo-Vacuum

In order to ensure the physical integrity of the LVPS subsystem in sub-orbital flight conditions (upper atmosphere), a series of thermo-vacuum tests have been conducted in a custom-made vacuum chamber with thermal control. The chamber uses a mechanical pump in order to reach the minimum pressure conditions.

The experimental instrument has a volume of roughly 60L, inside which an aluminum plate (30 cm × 30 cm × 1 cm) is resting on 4 stainless steel

rods. The aluminum plate is connected to a refrigerator, which allows cooling down to −37 °C. A heater, made of NiCr, attached to the surface of the plate, is used to regulate the aluminum plate temperature in the range from −37 °C to +80 °C. In addition to the mechanical pump, if required, a second turbo pump stage can be used to reach 10^{-6} Torr. However, the most demanding test for the system is at the higher pressure of 3 mbar, where thermal conduction is highly reduced and convection is negligible, but there is still enough air in the rarefied atmosphere to produce unhindered sparks.

The test results will warrant the operation of LVPS modules in vacuum environment (3 mbar), for temperatures ranging from −20 °C to +50 °C, validating the overall thermal requirements imposed to the EUSO balloon experiment. The baseline duration time of the first flight of the EUSO-balloon is approximately 12 hours. Furthermore, at the moment all the phases of balloon ascension cannot be simulated with the current experimental setup owing conditions of humidity and radiation exposure are not implemented for performing inside vacuum jar.

Therefore, a series of tests comprising module on/off activation, constant full load operation, V&I monitoring information, status relay and temperature monitoring were conducted over a period beyond 12 hours in vacuum conditions in compliance with [20], [21]. Figure 22 shows the setup for testing LVPS modules, already mounted in the provisional euro rack structure, at constant full load.

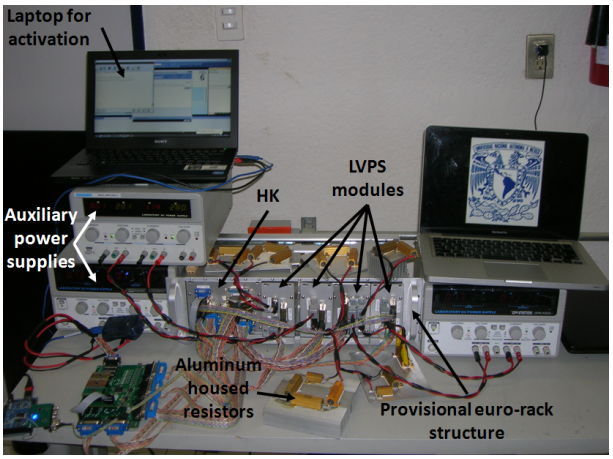

Fig. 22: Set-up for testing LVPS modules outside vacuum chamber.

On other hand, Fig. 23 shows an electronic setup with the four LVPS modules and HK system housed in the same rack. The HK was used both, through its regular interface with the LVPS subsystem, and as a probe inside vacuum for testing temperatures at several critical components of the LVPS modules. Input power twisted supply cables from two main laboratory power supplies were used to bias LVPS modules through 28 V bus voltage. Meanwhile, differential cables from monitoring LVPS connectors (twisted color cables in figure above) come out for transmitting to HK unit. Furthermore, twisted output power cables from 14 AWG to 20 AWG gauge were connected to fixed value aluminum housed power resistors which were calculated in order to demand full load operation. Finally, three thermistors at most critical and power demanded DDCU were located: one at CPU, and 2 at DST section.

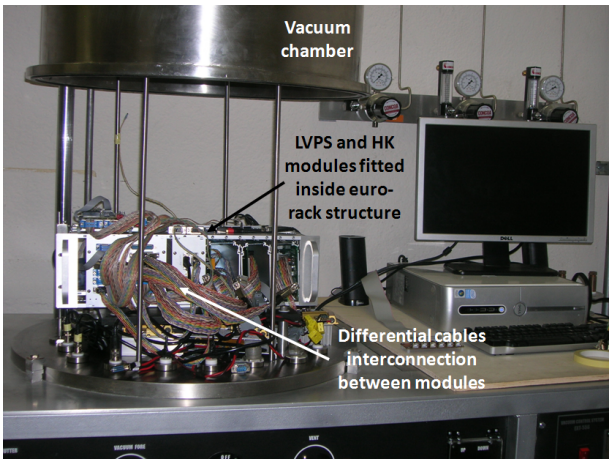

Fig. 23: Set-up for testing LVPS modules inside vacuum chamber.

As was mentioned above in thermal management section, as a first test, was implemented a setup (at room temperature ∼ 25 °C) which helps basically to know three aspects. The first one was the measurements (at full load) from current monitoring circuits. Table 6 shows the measurements according to each subsystem. These values were acceptable regarding cable length losses.

Tab. 6: DDCU monitored current measurements at full load.

Subsystem	Experimental current load (A)	Current monitoring (A)
CCB	1	0.982
CLKB	0.793	0.971
GPRS	0.357	0.347
PDM FPGA	2	1.95
PDM EC-ASIC	3	1.97
CPU	1	0.988
DST	3	2.89
HK-MCU	N/A	0.107
HL-LVDS	N/A	0.183

The second aspect was in order to be sure about similar current consumption of parallel configuration comprised by two DDCU of DST section (see Fig. 10(a)). Consequently, temperature rise of both converters was monitored. As can be seen in Fig. 24, the tempera-

ture difference between both converters (DC/DC1 and DC/DC2) before 15 min was less than 2 °C), which is acceptable. After that, the difference increase which probably indicates an unbalanced load operation.

The third reason was in order to figure out how long it takes to reach ∼ 85 °C (maximum case temperature). Approximately in 20 min both converters reach the temperature barrier. Therefore, in order to decrease the temperature on converters, the HS manufactured and implemented in LVPS2-DP module (see Fig. 10(c)) was used as a part of the setup showed in Fig. 25. This setup comprise HK subsystem, using through its regular interface with LVPS subsystem and as a probe for testing temperatures of LVPS components; and two LVPS modules, LVPS2-DP and LVPS-HK, the last powering HK subsystem. The LVPS2-DP module was fixed in vertical position, in that way, the rear side of HS (coming out from LVPS2-DP module) was in direct contact with aluminum plate of vacuum jar and the heat transfer between them was improved by using thermal grease. A set of thermistors were implemented as was described previously. Furthermore, two more thermistors were added, one on HS over the edge (HS and aluminum plate boundary contact) and other on aluminum plate. This test was done at room temperature inside of vacuum jar (not functioning) with the main aim to compare the thermal performance over 20 min.

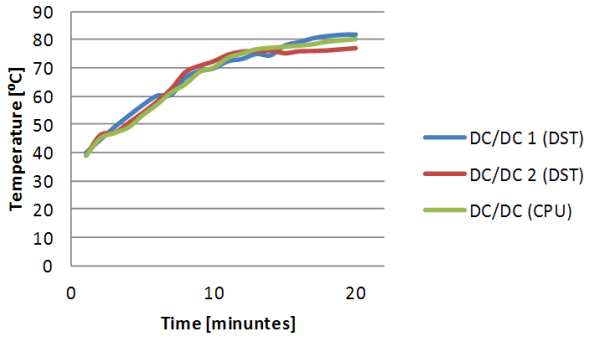

Fig. 24: Rise temperature of DST section DDCU on LVPS2-DP module.

The result was that temperature decreases at 35 °C in 20 min which represent an improvement on LVPS module thermal performance. However, it is necessary to perform a longer test under environmental conditions of Balloon project. Therefore, in order to continue the module test, vacuum jar was closed and pressure ambient was set at 3 mbar. The module performance continued working during 90 min in which temperature was reaching ∼ 55 °C as can be observed at Fig. 26.

Finally, keeping the same pressure conditions and the setup of Fig. 25, the LVPS2-DP module was subjected to two thermal increments at the plate (the

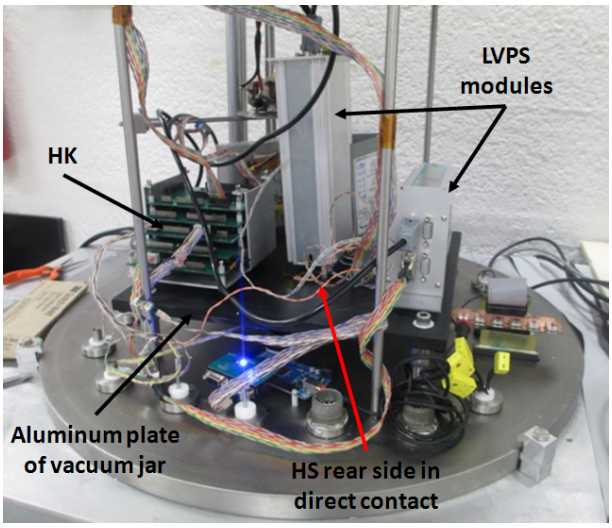

Fig. 25: Thermal performance test of DDCU of LVPS2-DP module at room temperature.

amount of thermal steps is shown in Fig. 27, Fig. 28 and Fig. 29, in blue line) through heater located under aluminum plate.

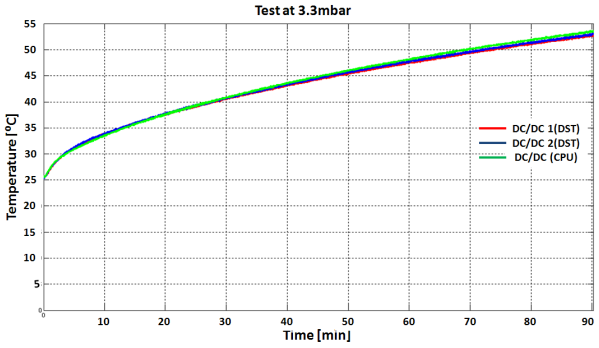

Fig. 26: Thermal performance of LVPS2-DP converters at 3 mbar conditions.

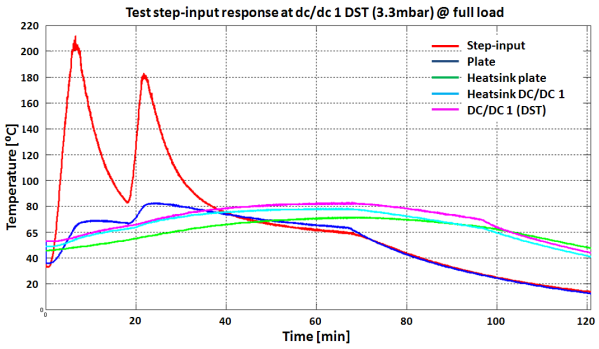

Fig. 27: Thermal performance of LVPS2-DP DDCU1 of DST section.

The last was done with the main aim to figure out the converters behavior when reach the maximum case temperature considering those environmental conditions provided by vacuum jar. The red curve describes

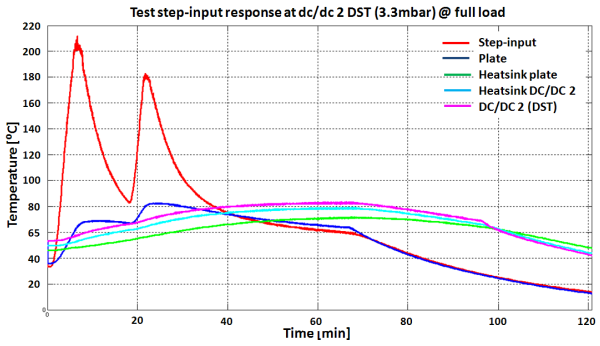

Fig. 28: Thermal performance of LVPS2-DP DDCU2 of DST section.

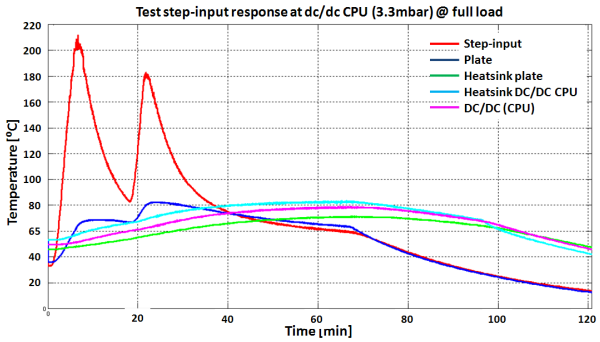

Fig. 29: Thermal performance of LVPS2-DP DDCU of CPU section.

the thermal steps in heater (attached to plate) providing those two increments in aluminum plate; meanwhile green line describes the temperature at the edge of HS and plate. The remaining two lines, light-green and purple, describe the rise temperature at heat sink (on DDCU) and lateral side case of DDCU under test, respectively. Therefore, Fig. 27, Fig. 28 and Fig. 29 describe, in separately way, the thermal performance over 120 min of three DDCU of LVPS2-DP module.

Consequently, in figures above can be observed that maximum case temperature after 60 min of continuous performance (at full load approximately) is reached. Also, is important to mention that load conditions test are not the same of real performance of subsystems balloon. However, the tests here described and performed have the main aim to characterize the LVPS modules under WC conditions.

Finally and, getting advantage of final integration phase of EUSO-Balloon project at INFN-Naples, Italy, LVPS modules were tested under real load and environmental balloon conditions with all subsystems. However, DST section power consumption was higher than specified causing an extra heating on DDCU of DST section on LVPS2-DP module. This inconvenient was resolved attaching the heat sink (of power module) to cooling plate of DP rack in order to increase surface heat dissipation. Figure 30 shows how temperature is stabilized, at 51 °C, after reach 10 hrs of continues working. This temperature does not represent danger on DDCU performance.

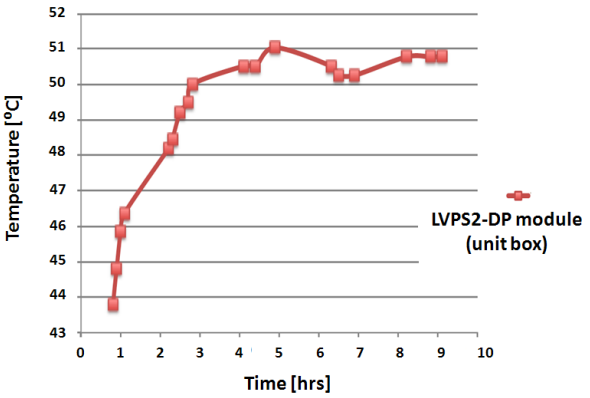

Fig. 30: Thermal performance of LVPS2-DP module during final integration test in Naples, Italy.

8.4. Weight

Weight is often a critical issue in every payload of space and sub-orbital project. Therefore, Tab. 7 shows how each module of LVPS subsystem meet the requirements regarding weight constrain. Furthermore, weight of-provisional rack structure is also included in Tab. 7.

Tab. 7: Weight of each LVPS subsystem modules.

Subsystem	Weight (kg)
LVPS-PDM	0.9
LVPS1-DP	1
LVPS2-DP	0.9
LVPS-HK	0.9
Sub-total	**3.7**
Rack	1.3
Total	**5**

9. Conclusion

A fully operational low-voltage power supply subsystem has been developed for a sub-orbital EUSO-Balloon instrument. The LVPS subsystem has the capability to operate at 3 mbar pressure environment under maximum load current consumption in a temperature range from −20 °C to +50 °C. The subsystem comprises four power modules which can be remotely activated, in reliable way, through 12 V HL_CMD pulses provided by external subsystems, HK and SIREN. The four modules developed provide isolation between 28 V main power bus and secondary power bus to payload users, avoiding failures propagation. At same time, the modules provide voltage

transformation to low-voltage levels ±12 V, 5 V, 5.5 V and 3.3 V, allowing to implement tight regulation stage ($\leq \pm 1$ %) on-board subsystems by the use of linear regulators or niPoL. The modules are able to withstand low excursion voltage level from PWP (from 18 V to 30 V) and provide 10 % tolerance on output voltage levels (secondary power bus).

Regarding environmental conditions, importance level of some subsystems, and considering that EUSO-Balloon is a recoverable instrument (future flights planned) the LVPS modules provide I/O short circuit protection by the use of fuse at input, over-temperature protection, and since the switching power supplies are the major EMI noise contributors on instrument, I/O EMI filters were implemented (according to manufacturer specifications) in order to minimize the instrument contamination by conducting interference from tracks, connectors, cables, etc.

Additionally, PCB power modules were enclosed into individually unit boxes with the main aim to minimize the radiated interference and, at the same time, be less susceptible to external EMI. Another capability of LVPS subsystem consists of providing voltage and current levels information (proportionally to 0 V to 5 V output range monitoring circuits) as TM data to HK. Furthermore, the power modules allow verification status of LR's clamps in order to control reliable power supply to each subsystem. The power modules also comply with the Eurocard size dimensions, and consequently, meet the weight restriction imposed at requirements section, ≤ 5 kg.

Thermal management was a complicated issue. A heat sink of $\theta_{SA} = 5.68\,^{\circ}\mathrm{C/W}$ was manufactured in order to provide an extra path conduction dissipation for LVPS2-DP, which did represent the most critical module related to thermal performance. Stable thermal performance of 51 °C was obtained attaching HS designed to DP cooling plate.

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